SE311: Design of Digital Systems

Lecture 9: NAND and NOR Implementations

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(Term 041)

Outlines

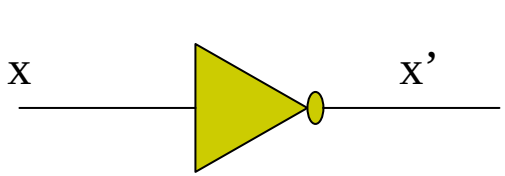
- NAND and NOR Implementations
- two level Implementations
- Multi-level NAND circuits
- NOR Implementations
- Other Two level implementations
- Exclusive OR Function
- Parity Checking

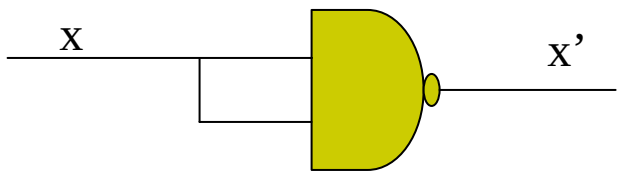
NAND and NOR Implementations

- Digital circuits are often implemented using NAND or NOR gates rather than AND-OR gates
- NAND or NOR gates are
  - Easier to manufacture
  - Universal gates (can be used to implement to logic function)
  - They are the basic gates in IC digital families

NAND Gate is a Universal Gate

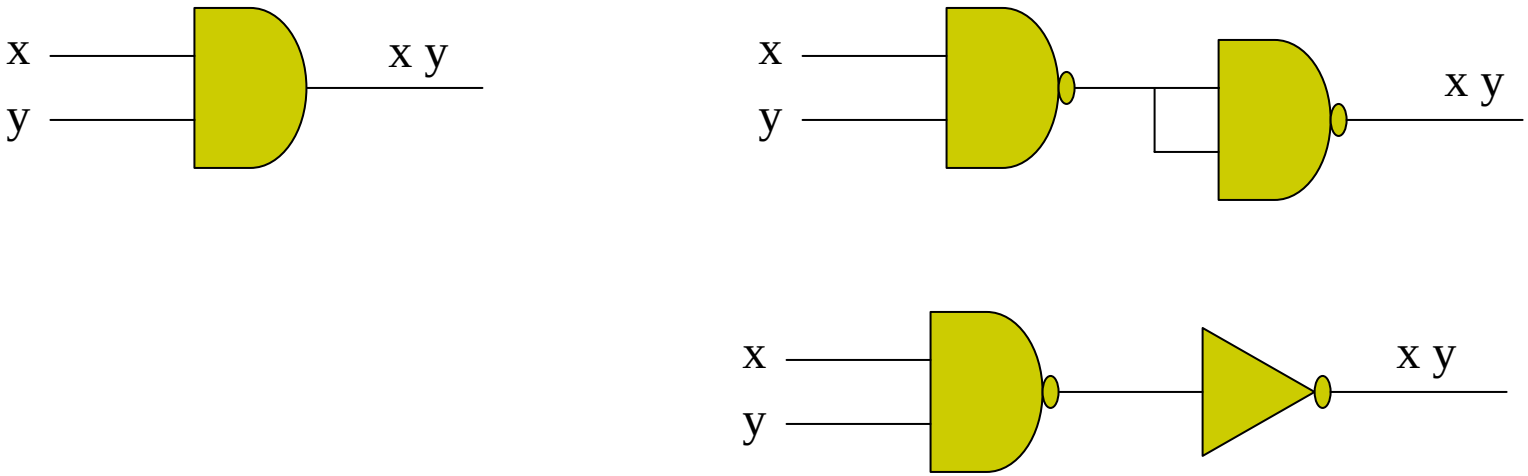
- We can use NAND gates to implement any Boolean function
- We can implement ant function using AND, OR, NOT and we will show that we can implement them using NAND gates





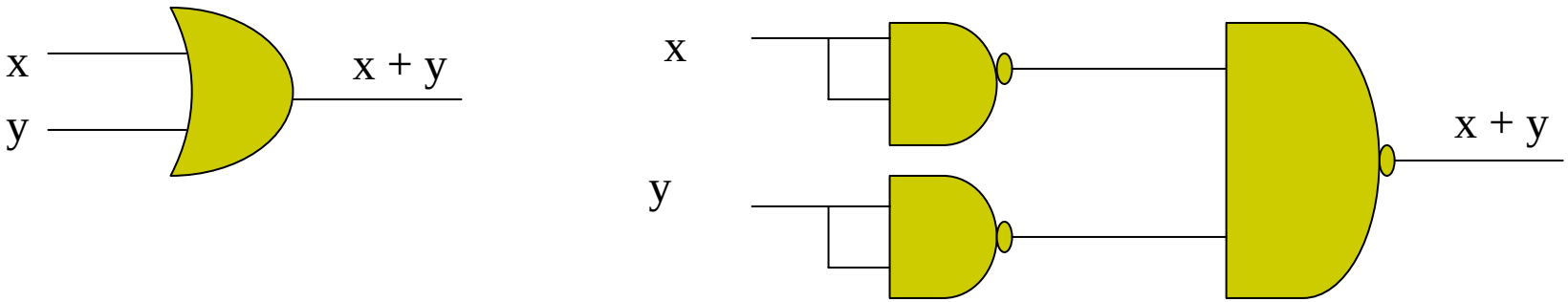
We often use this symbol to represent the single input NAND gate

NAND Gate is a Universal Gate



AND operation can be implemented using NAND gated

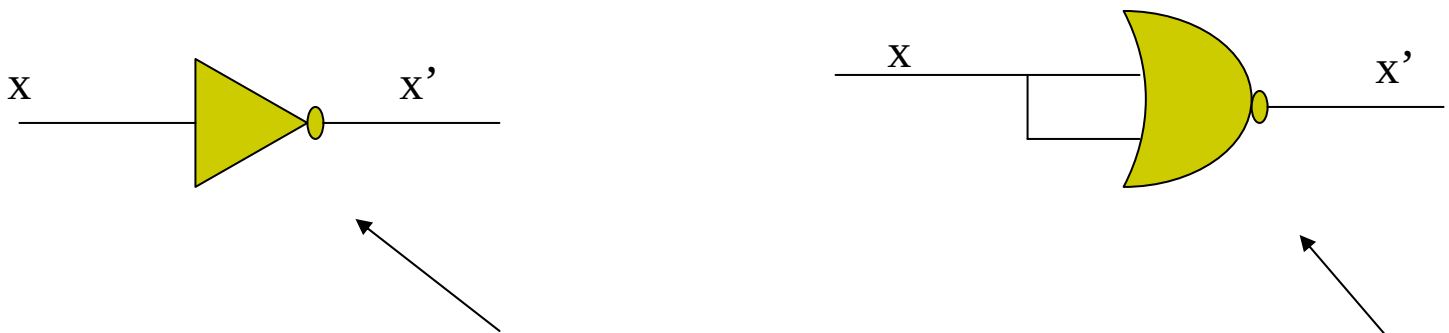
NAND Gate is a Universal Gate



OR operation can be implemented using NAND gated

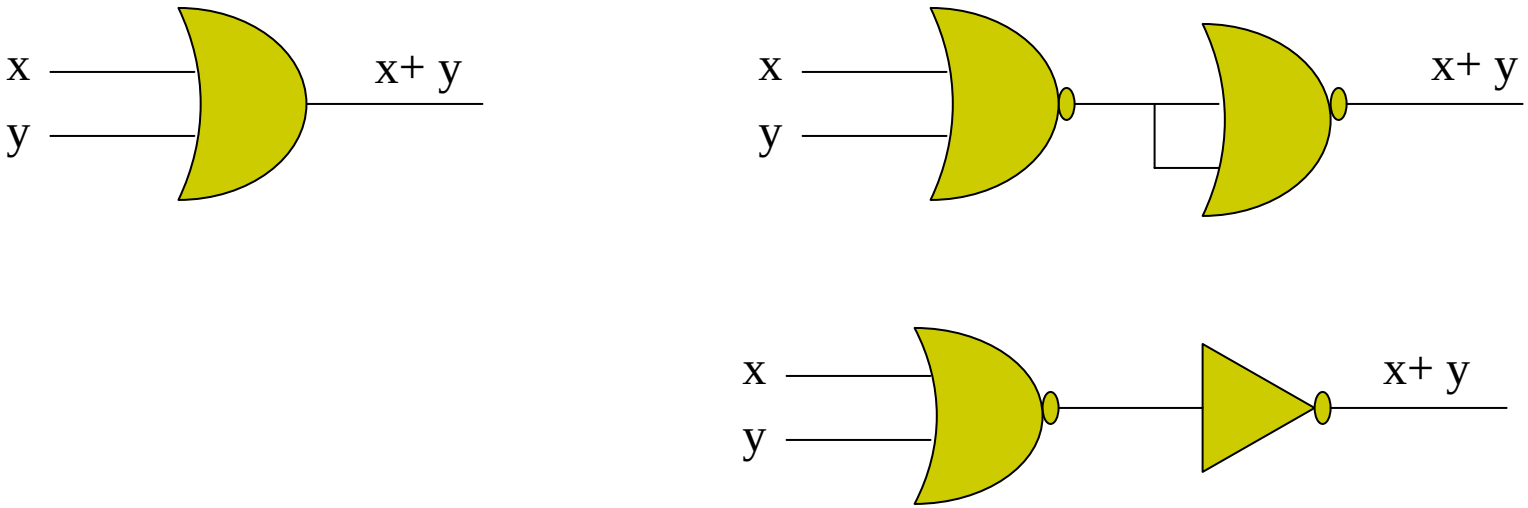
NOR Gate is a Universal Gate

- We can use NOR gates to implement any Boolean function
- We can implement AND, OR, NOT using NOR gates



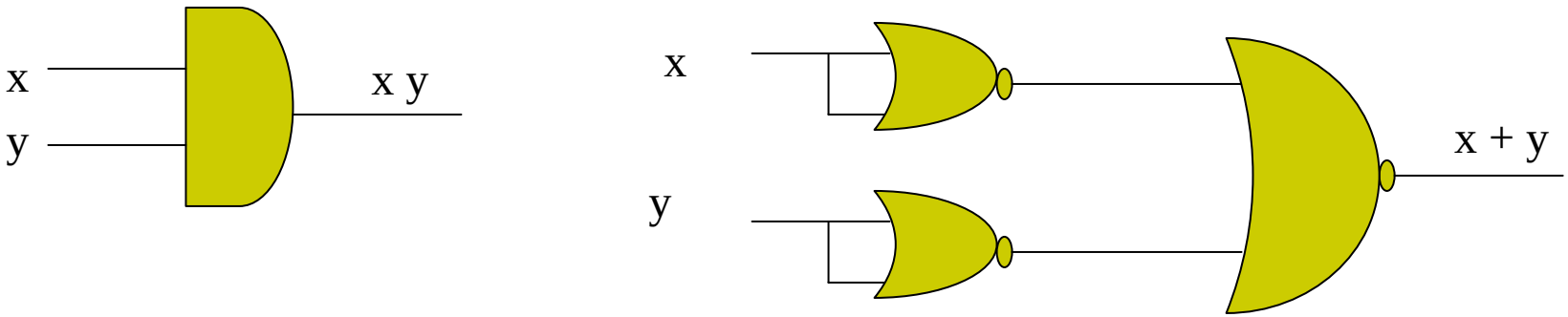
We often use this symbol to represent the single input NOR gate

NOR Gate is a Universal Gate



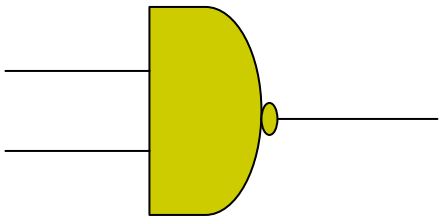
OR operation can be implemented using NOR gates

NAND Gate is a Universal Gate



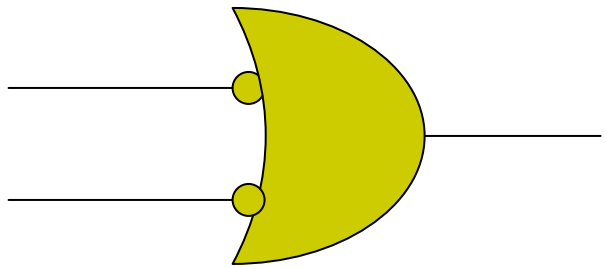
AND operation can be implemented using NOR gates

NAND Circuits



Standard symbol for NAND gate

(AND-Invert)



Alternative symbol for NAND gate

(Invert-OR)

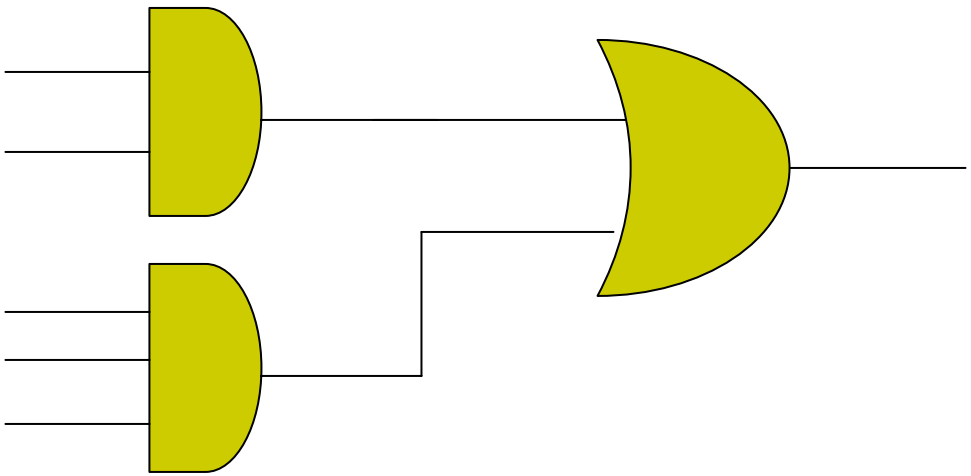
NAND gate Implementations

- Any Boolean function can be implemented using 2-level NAND gates

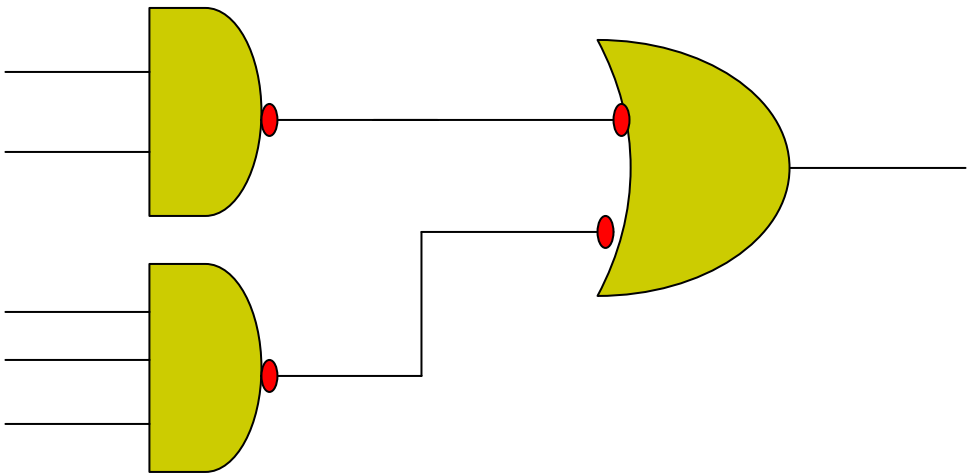
Procedure:

1. Simplify F(.) as the sum of product form
2. Draw NAND gate for each term that has two literals or more.
3. Draw a single gate using AND-invert or Invert-OR in the second levels with inputs coming from first level.
4. A single literal term needs inverter in the first level (unless it appears in the complement form)

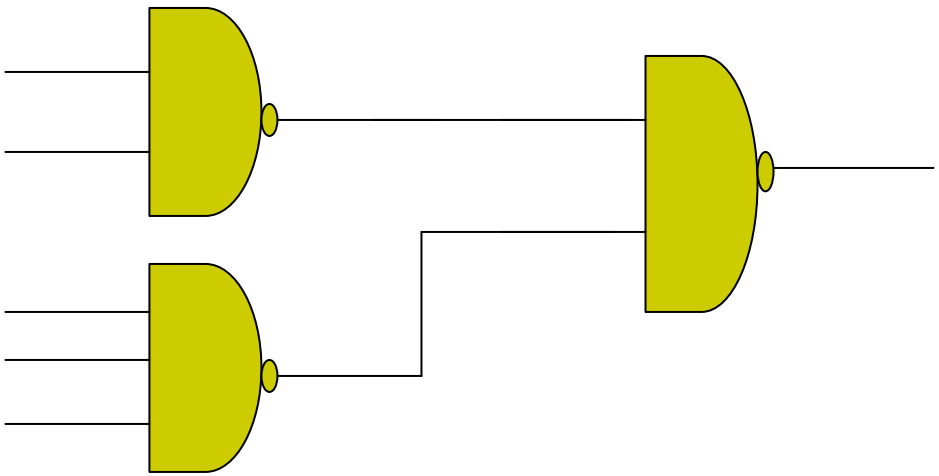
Implement using NAND gates



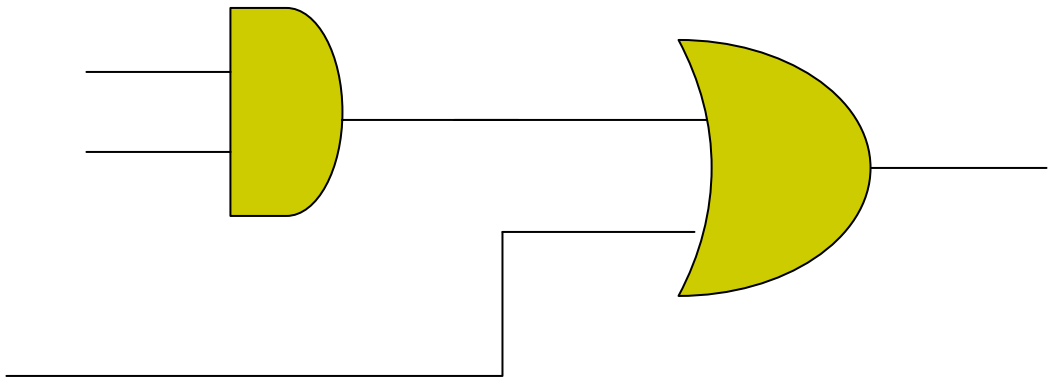
NAND Circuits



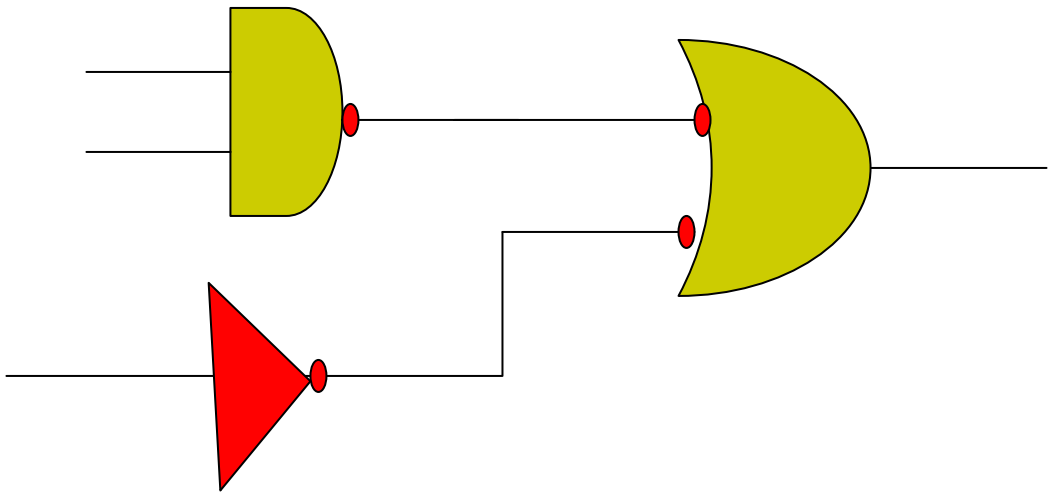
NAND Circuits



Implement using NAND gates



Implement using NAND gates



Summary

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- two level Implementations
- Multi-level NAND circuits
- NOR Implementations
- Other Two level implementations
- Exclusive OR Function
- Parity Checking