Ref: Online course on EE-390, KFUPM

Handout 15

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Memory Interface of 8088 and 8086 processors

Objective:

- To introduce the read and write bus cycles of the 8088 and 8086 processors.
- To discuss timing states associated with read/write bus cycles

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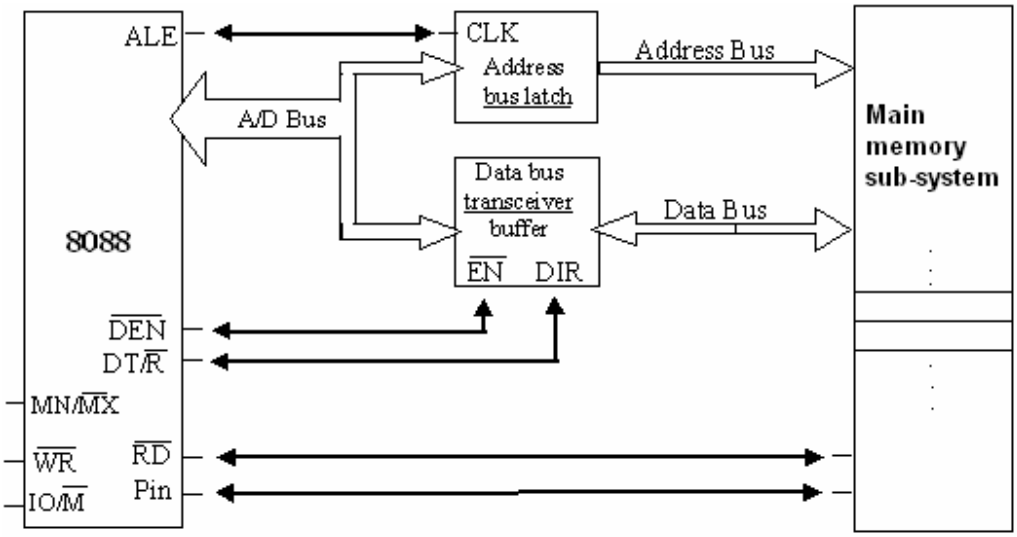
Slide 1: **Memory interface of a Minimum-mode 8088 system:**

- The block diagram below represents a memory interface circuitry of an 8088 based system, operating in minimum mode.



- **Note:** Note that aside from the CPU (8088) and the memory-subsystem, the main components of this diagram are “Address bus latch”, “Data bus transceiver buffer” and address and data buses.
- The address bus carries the physical address generated by the CPU and selects the memory location to be accessed. The control signals (ale, read, write ….) are also shown in the diagram.
- The data bus transfers data between the CPU registers and the selected memory location

Slide 2: **Timing Status of Minimum-mode 8088 memory interface:**

- Since a memory read or write should be complete within one bus-cycle (4-CLK pulses, T_1 -T_4), related timing states as follows:
  - T_1 *(speech only: or the 1st clock pulse)*- starts the bus cycle. Actions include setting control signals to give the required logic values for IO/M, ALE, DT/R and a valid address onto the address bus.
  - T_2 - the $\overline{RD}$ or $\overline{WR}$ control signals are issued, $\overline{DEN}$ is asserted and in the case of a write, data is put onto the data bus. The $\overline{DEN}$ turns on the data bus buffers to connect the CPU to the external data bus. The READY input to the CPU is sampled at the end of T_2 and if READY is low, wait state (T_W) is inserted before T_3 begins.
  - T_3 - this clock period is provided to allow memory to access the data. If the bus cycle is a read cycle, the data bus is sampled at the end of T_3 or the 3rd clock pulse of the bus-cycle.
  - T_4 - all bus signals are deactivated in preparation for the next clock cycle. The 8088 also finishes sampling the data (in a read cycle) in this period. For the write cycle, the trailing edge of the WR signal transfers data to the memory.

Slide 3: **Minimum-mode Memory-Read bus-cycle of 8088 system:**

- To complete the minimum-mode memory-read bus-cycle, the required control signals with appropriate active logic levels are :
  - IO/$\overline{M}$ = ‘logic 0’, to select memory interface
  - MN/$\overline{MX}$ = ‘logic 1’, to select minimum-mode of operation
  - DT/$\overline{R}$ = ‘logic 0’, to activate the data-receive mode of ‘Data-bus-buffer’
  - Valid Physical-address of memory-location via address-bus (A_{19} to A_0)
  - ALE-pulse, to latch the valid Physical-address. (⎍⎍)
  - $\overline{RD}$ = ‘logic 0’, to initiate reading data into CPU. Note, $\overline{WR}$ = ’logic 1’
  - $\overline{DEN}$ = ‘0’, enables the ‘Data-Bus-transceiver-buffer’ to let data pass
  - Reset $\overline{RD}$=$\overline{DEN}$=’logic1’, to END the read-bus-cycle.

- Memory interface block diagram related to above steps are shown in slide 1

Note: Next slide illustrates the timing diagram of these control signals

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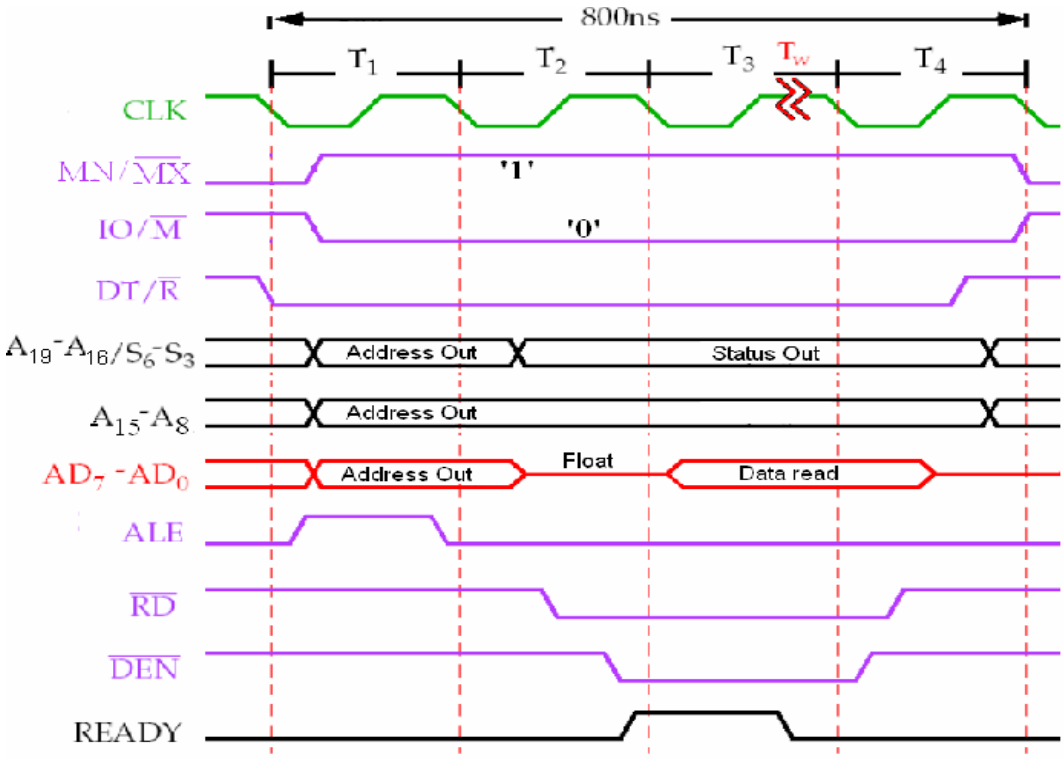
Slide 4: **Minimum-mode Memory-Read cycle of 8088 (Cont'd):**

- The timing diagram for 8088 minimum mode memory read operation is shown below using logic '0' and '1' waveforms.



Note: *Note that during T_1 or the 1st clock pulse, the read bus cycle startes and valid address is latched together with setting minimum and maximum mode, input output or memory interface, data transmit and receive mode of buffer IC.*

During T_2 , the Read control signals are issued and data enable signal is asserted. Note that during this state the READY signal is also checked to insert wait status, if needed

During T_3 , the data from the memory is read by sampling the data bus at the end of T_3

During T_4 , all bus signals are deactivated in preparation for the next clock cycle.

Slide 5: **Minimum-mode Memory-Write bus-cycle of 8088 system:**

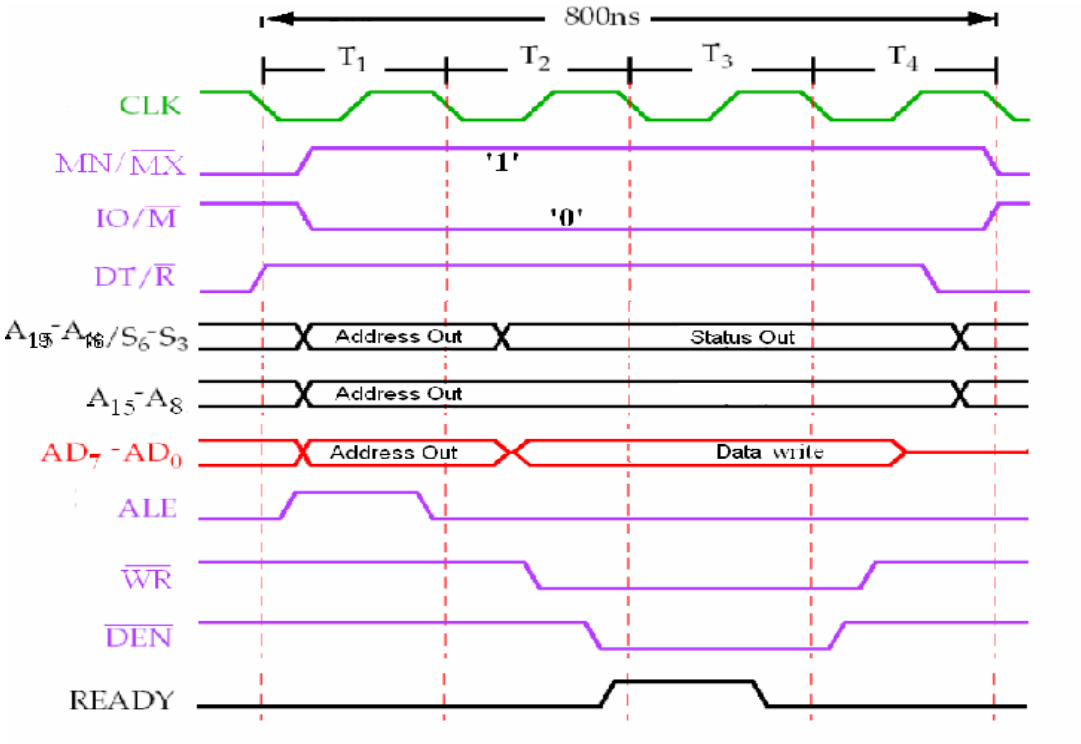
- To complete the minimum-mode memory-write bus-cycle, the required control signals with appropriate active logic levels are :
  - IO/$\overline{M}$ = ‘logic 0’, to select memory interface
  - MN/$\overline{MX}$ = ‘logic 1’, to select minimum-mode of operation
  - DT/$\overline{R}$ = ‘logic 1’, to activate the data-transmit mode of ‘Data-bus-buffer’
  - Valid Physical-address of memory-location via address-bus (A_{19} to A_0)
  - ALE-pulse, to latch the valid Physical-address. (⎍⎍)
  - $\overline{WR}$ = ‘logic 0’, to initiate memory data writing. Note, $\overline{RD}$ = ’logic 1’
  - $\overline{DEN}$ = ‘0’, enables the ‘Data-Bus-transceiver-buffer’ to let data pass
  - Reset $\overline{WR}$=$\overline{DEN}$=’logic1’, to END the write-bus-cycle.

- Memory interface block diagram related to above steps are shown in slide 1

Note: In the next slide, the timing diagram of these control signals are explained

Slide 6: **Minimum-mode Memory-Write cycle of 8088 (Cont'd):**

- The timing diagram for 8088 minimum mode memory write operation is shown below using logic '0' and '1' waveforms.

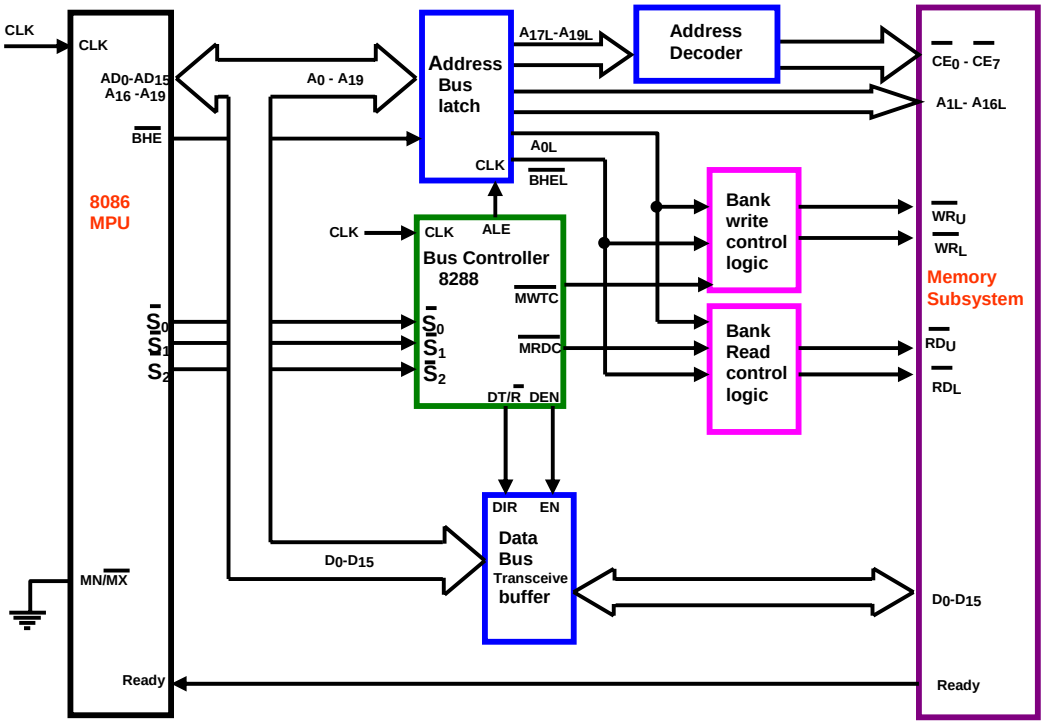


Note: *Note that the control signal logic levels and timing diagram are similar to that of read operation, except for data transmit or receive mode, read and write signals.*

The response of the ready signal is not shown here, as it behaves in the same way as data read process.

Slide 7: **Memory interface of a Maximum-mode 8086 system:**

- The block diagram below shows the memory interface circuit of an 8086 based system operating in maximum mode.



Note: The Bus controller is introduced here due to the support of multiprocessor environment of Maximum mode. The decoder is used to select desired memory chips. The remaining components of this circuit are similar to 8088 minimum mode circuit, as shown in slide 1.

Note that the bank high enable signal is used to control the access of even or odd memory banks of 8086 system. Also, the difference in the required logic level for data enable signal in maximum and minimum mode is visible by comparing this figure with the figure of slide 1

Slide 8: **8288 Bus-controller for 8088/8086 Maximum-mode:**

- The status codes ($\overline{S_0}$,$\overline{S_1}$,$\overline{S_2}$) of the CPU is used by the bus-controller to activate maximum mode memory control signals:

Status Inputs			CPU Cycle	8288 Command
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

- These codes are important for multiprocessor environment, supported by Maximum mode.

Slide 9: **Maximum-mode Memory-Read bus-cycle of 8086 system:**

- To complete the minimum-mode memory-read bus-cycle, the required control signals with appropriate active logic levels are :
  - IO/$\overline{M}$ = 'logic 0', to select memory interface
  - MN/$\overline{MX}$ = 'logic 0', to select maximum-mode of operation
  - DT/$\overline{R}$ = 'logic 0', to activate the data-receive mode of 'Data-bus-buffer'
  - Valid Physical-address (A_0 to A_{19}) and $\overline{BHE}$ signal is generated by CPU
  - ALE-pulse, to latch the valid Physical-address. (⎍⎍)
  - Proper status code $\overline{S_0}$ to $\overline{S_2}$ (as shown in table of slide 8) is generated by CPU to initiate data reading ($\overline{MRDC}$) from the desired memory bank
  - DEN = '1', enables the 'Data-Bus-transceiver-buffer' to let data pass
  - Reset $\overline{MRDC}$ and DEN signals to END the read-bus-cycle.

- *Memory interface block diagram relating to these signals are shown in slide 7*

Note: In the next slide, the timing diagram related to these control signals are illustrated

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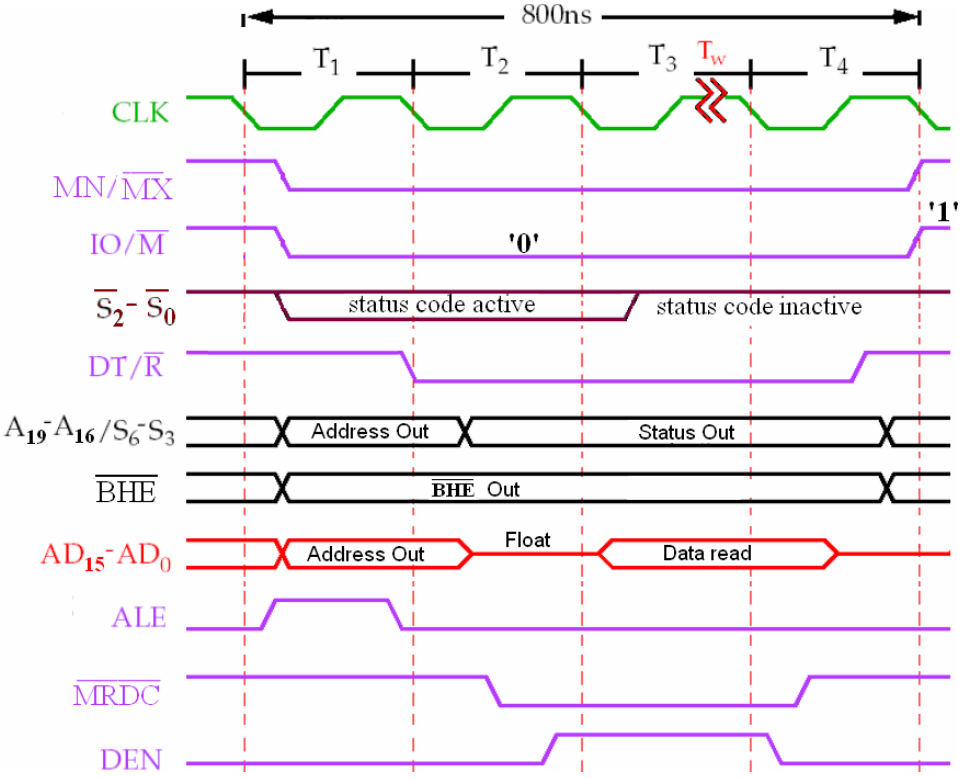
Slide 10: **Maximum-mode Memory-Read cycle of 8086 (Cont'd):**

- The timing diagram for 8086 maximum mode memory read operation is shown below using logic '0' and '1' waveforms.



Note: *Note that in maximum mode status codes needs to be active to generate control signals from bus controller.*

The logic level required for BHE signal to access even and odd banks are discussed in earlier lecture.

Slide11: **Maximum-mode Memory-Write bus-cycle of 8086 system**

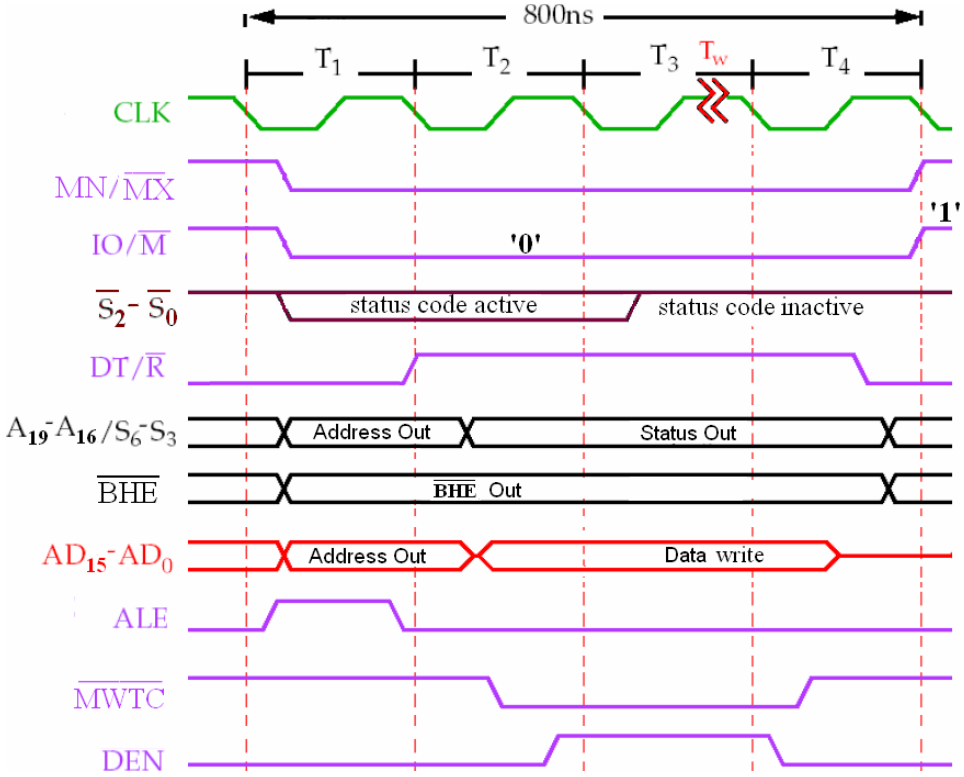
- To complete the maximum-mode memory-write bus-cycle, the required control signals with appropriate active logic levels are :
  - IO/$\overline{M}$ = 'logic 0', to select memory interface
  - MN/$\overline{MX}$ = 'logic 0', to select maximum-mode of operation
  - DT/$\overline{R}$ = 'logic 1', to activate the data-transmit mode of 'Data-bus-buffer'
  - Valid Physical-address (A_0 to A_{19}) and $\overline{BHE}$ signal is generated by CPU
  - ALE-pulse, to latch the valid Physical-address. (⎍)
  - Proper status code $\overline{S_0}$ to $\overline{S_2}$ (as shown in table of slide 8) is generated by CPU to initiate data writing (MRTC) from the desired memory bank
  - DEN = '1', enables the 'Data-Bus-transceiver-buffer' to let data pass
  - Reset $\overline{MRTC}$ and DEN signals to END the read-bus-cycle

- *Memory interface block diagram relating to these signals are shown in slide 7.*

Note: In the next slide, the timing diagram relating to these control signals are explained

Slide 12: **Maximum-mode Memory-Write cycle of 8086 (Cont'd):**

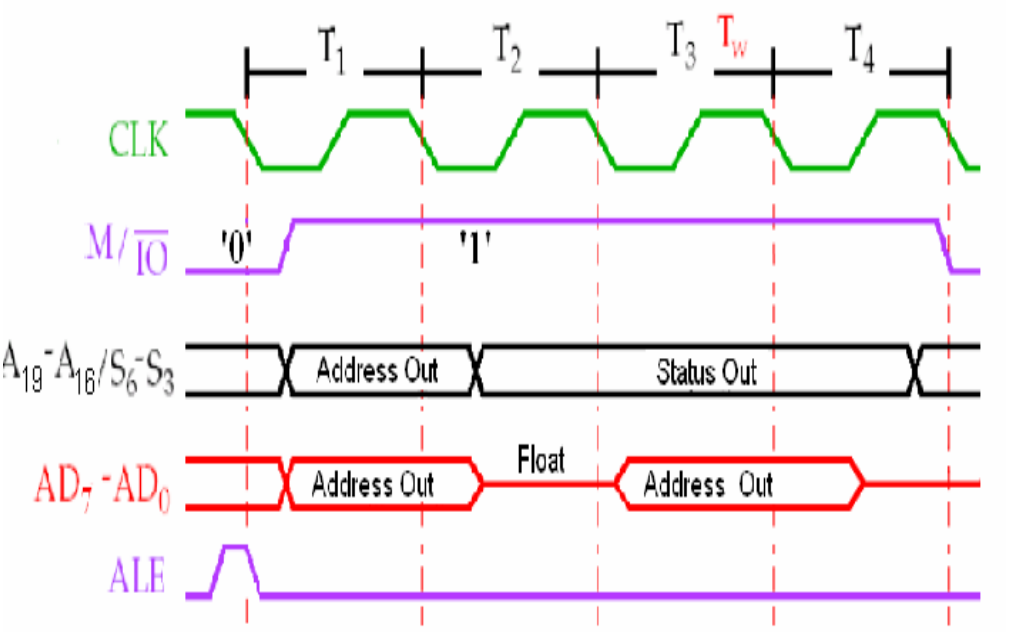
- The timing diagram for 8086 maximum mode memory write operation is shown below using logic '0' and '1' waveforms.



Note: *Note that the control signal logic levels and timing diagram are similar to that of read operation, except for data transmit and receive, memory read and write signals.*

Slide 13: **Example 1:**

For the given timing diagram of a **8088 memory read bus-cycle, find the errors** in the diagram and indicate them in the given boxes (*T1 - T4 are clock pulses that constitute one bus-cycle*)



WRITE below: **Correct** or **Incorrect**

(a)

(b)

(c)

(d)

Solution: (a) Incorrect, as 8088 processors IO/$\overline{M}$ signals, and require logic '0', for the duration of the bus-cycle, to activate the memory (read) interface.

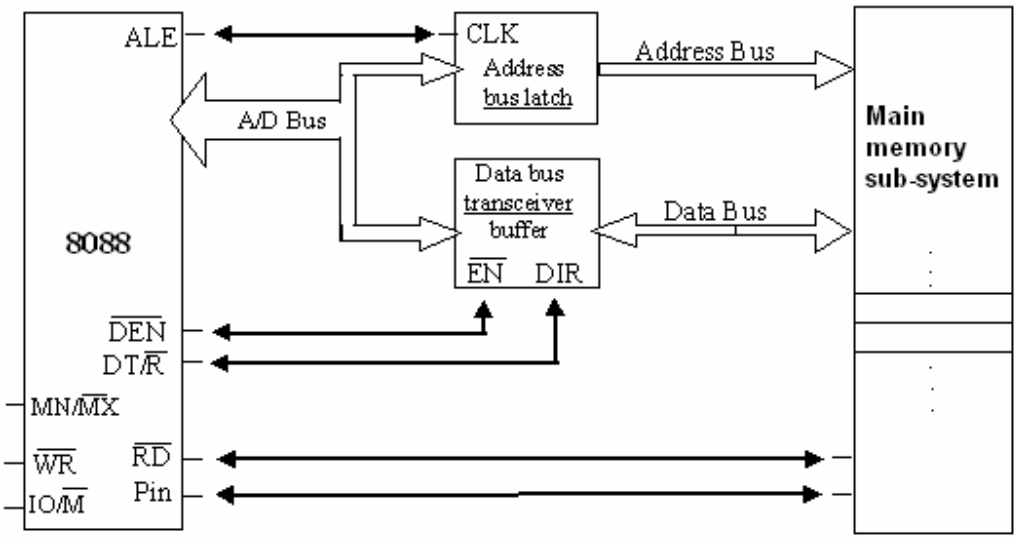
(b) Correct, as these multiplex pins (A_{19}-A_{16}/S_6-S_3) of 8088 processor has to generate valid physical address during the 1st part of the bus-cycle and then produce proper status codes during the remaining of the bus-cycle.

(c) Incorrect, as these multiplex pins (AD_7-AD_0) 8088 processors needs to access the data, to be read, during the 2nd half of the bus-cycle.

(d) Incorrect, as the falling-edge of the ALE pulse should occur when all the address pins (A_{19}-A_0) carry valid physical address. (note that although the response of (A_{15}-A_8) are not shown, it is assumed that it will carry valid P.A. during 1st part of the bus-cycle)

Slide 14: **Example 2:**

For the given figure below, if 8088 is performing a minimum mode memory write bus cycle, which logic levels must be applied to $\overline{DEN}$, DT/$\overline{R}$ and $\overline{RD}$ pins.



Solution:

(1) **DT/$\overline{R}$='1'** is send to activate transmit mode of "Data bus transceiver buffer IC"

(2) $\overline{RD}$ = '1' is send to de-activate data read process.

(3) $\overline{DEN}$ = '0' is send to enable the "Data bus transceiver buffer IC"

Slide 15: **Exercise:**

If the instruction "PUSH AX" is executed,

(a) what status-code ($\overline{S_0}$ to $\overline{S_2}$) is outputted by 8086 in Maximum mode

(b) what are logic levels of A_0 and $\overline{BHE}$?

(c) what read/write control signals are produced by bus-controller?

Sol: (a) $\overline{S_2}$='1', $\overline{S_1}$='1', $\overline{S_0}$='0'; (b) A_2='0'; $\overline{BHE}$='0' ; (c) $\overline{AMWC}$ and $\overline{MWTC}$