<u>Handout 3 for EE-203</u>

<u>Differential Amplifiers</u>

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<u>(Ref: Text book and</u>
<u>KFUPM Online course of EE-203)</u>

<u>(Remember to solve all the related examples,</u>
<u>exercises problems as given in the Syllabus)</u>

<u>Chapter 7</u> – Differential Amplifier

***<u>Reference</u>**: "Microelectronic Circuits by Sedra/Smith* and *EE-203 Online course, KFUPM*

- To discuss the basic operation, transfer characteristics, advantages, disadvantages and applications associated with differential amplifiers.

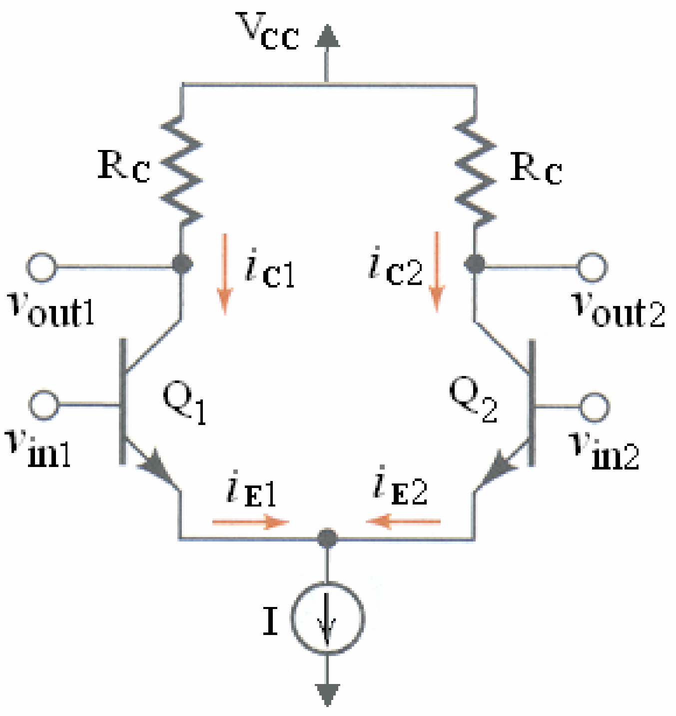
- Differential amplifier pair is a fundamental subcircuit used in the input stage of every operational amplifiers and many other linear integrated circuits.

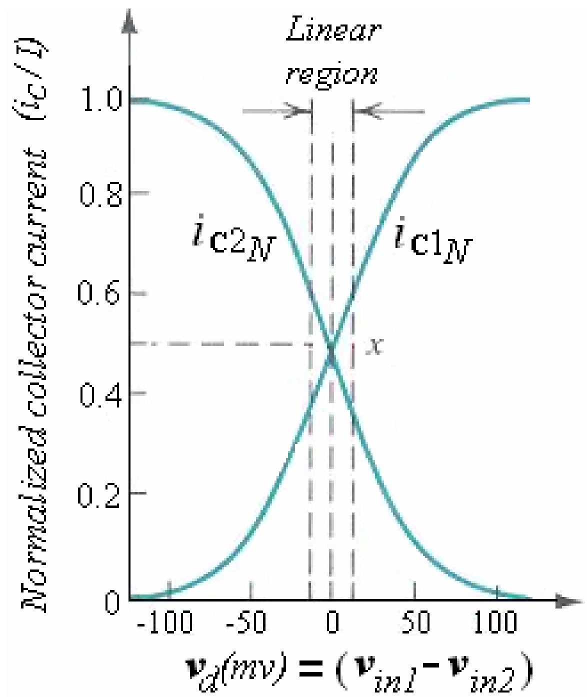
- Differential amplifier pairs can be constructed using Bipolar, MOS, BiCMOS and GaAs technologies, where GaAs makes possible the design of amplifiers having very wide bandwidths.

- Differential amplifier implemented using BJT (bipolar junction transistor) based differential pairs will be discussed in this section.

- Aside form differential amplifier, this BJT differential pair is also used to manufacture very high speed logic switches, called ECL logic gates. The operation of these gates will be discussed later in the class.

7.3: The BJT Differential Pair (D.P.):

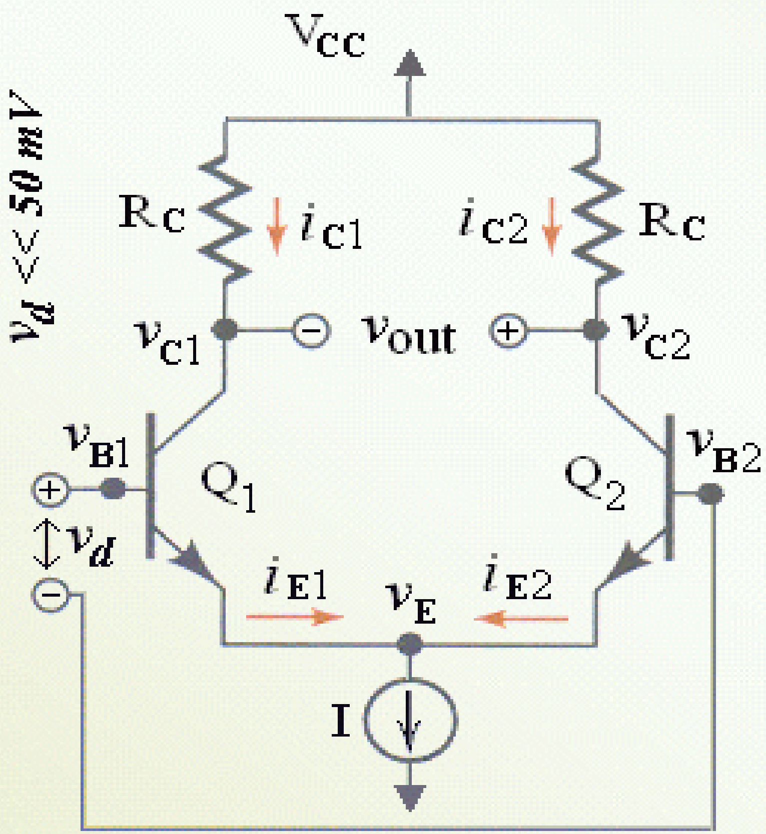




- The BJT differential pair, shown in the figure, consist of matched transistors Q1 and Q2, biased by a current source (I).
- Collector resistors are used to make sure, that, transistors never enters saturation.

- D.P. is also used as differential amplifier (*for very small differential input*), that has the ability to amplify wanted signals, while rejecting unwanted signals. Note, DP only works as an amplifier for small values of $v_d=(v_{in1}- v_{in2})$
- Note, DP behaves as linear amplifier for $|v_d|$ <20mV, when $v_{out}= v_{out1}-v_{out2}$
- Also, $v_d \approx 100\text{mV} = 4V_T$ is sufficient to switch the entire current (I) to any one side of the D.P., allowing it to be used as fast current switch (≈ ECL)

7.3.3: Small Signal Operation of BJT Differential Pair (D.P.):



For the given BJT differential pair;

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1}-v_E)/V_T} \text{ and } i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2}-v_E)/V_T}$$

since, $i_{E1}+i_{E2}=I$, **using eq 7.69, 7.70 of pg 707**

$$i_{E1} = \frac{I}{1+e^{-(v_d/V_T)}} \text{ and } i_{E2} = \frac{I}{1+e^{(v_d/V_T)}}$$

$$\text{and } i_{C1} = \frac{\alpha I}{1+e^{-(v_d/V_T)}}; \; i_{C2} = \frac{\alpha I}{1+e^{(v_d/V_T)}}$$

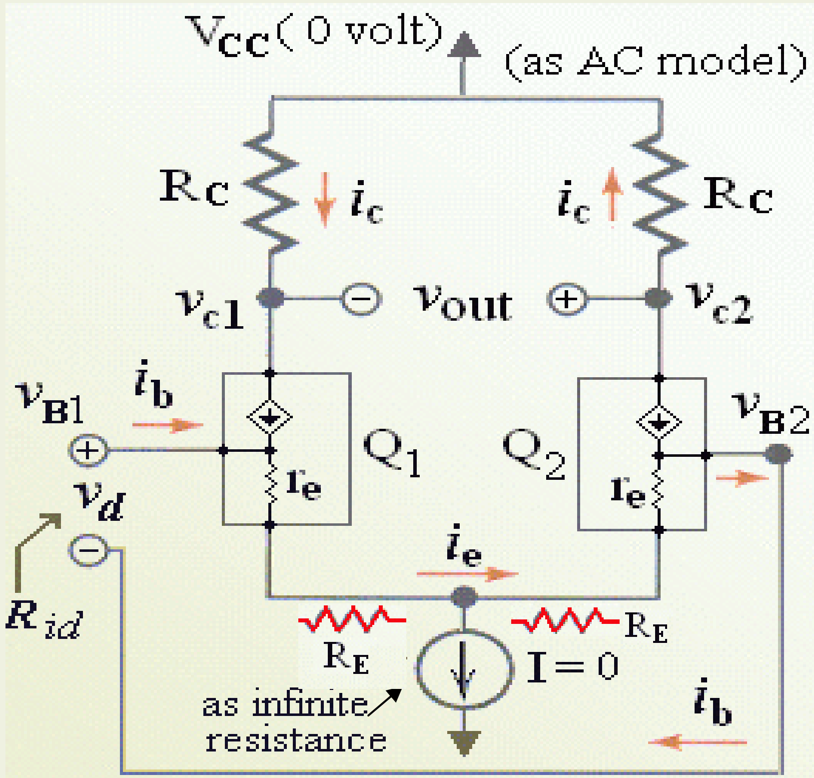
As shown in book pg 710, $i_{C1} = \frac{\alpha I}{2} + \left(\frac{\alpha I}{2V_T}\right)\left(\frac{v_d}{2}\right)$

or, $i_{C1} = \frac{\alpha I}{2} + \frac{g_m v_d}{2}$ where, $g_m = \alpha I/2V_T$

Thus, $v_{C1} = (V_{CC} - I_C R_C) - \left(g_m R_C \frac{v_d}{2}\right)$ (DC: $V_{CC} - I_C R_C$; AC: $g_m R_C \frac{v_d}{2}$)

Similarly, $i_{C2} = \frac{\alpha I}{2} - \frac{g_m v_d}{2}$

and $v_{C2} = (V_{CC} - I_C R_C) + g_m R_C \frac{v_d}{2}$. Thus for $v_d << (50mV \text{ or } 2V_T)$, the small signal (ac signal) differential gain is, $A_d = \frac{v_{c1} - v_{c2}}{v_d} = -g_m R_C = -\frac{\alpha R_C}{r_e}$



and the single ended differential gain is:

$$A_{ds} = \frac{v_{c1}}{v_d} = -\frac{g_m R_C}{2} = -\frac{\alpha R_C}{2r_e}$$

Now to find the input resistance of DA, its AC equivalent circuit is drawn. For ideal 'I' source, 'v_d' appears across '$2r_e$'

thus, $i_e = \dfrac{v_d}{2r_e}$ and since, $i_b = \dfrac{i_e}{(\beta+1)}$

$$R_{id} \equiv \frac{v_d}{i_b} = (\beta+1)(2r_e) = 2r_\pi$$

where 'R_{id}' is the input resistance of DA

For differential amplifier with emitter resistors, since the input signal is applied across resistance, (r_e+R_E);

$$i_e = \frac{v_d}{2(r_e+R_E)} \quad \text{and} \quad i_c = \frac{\alpha v_d}{2(r_e+R_E)}$$

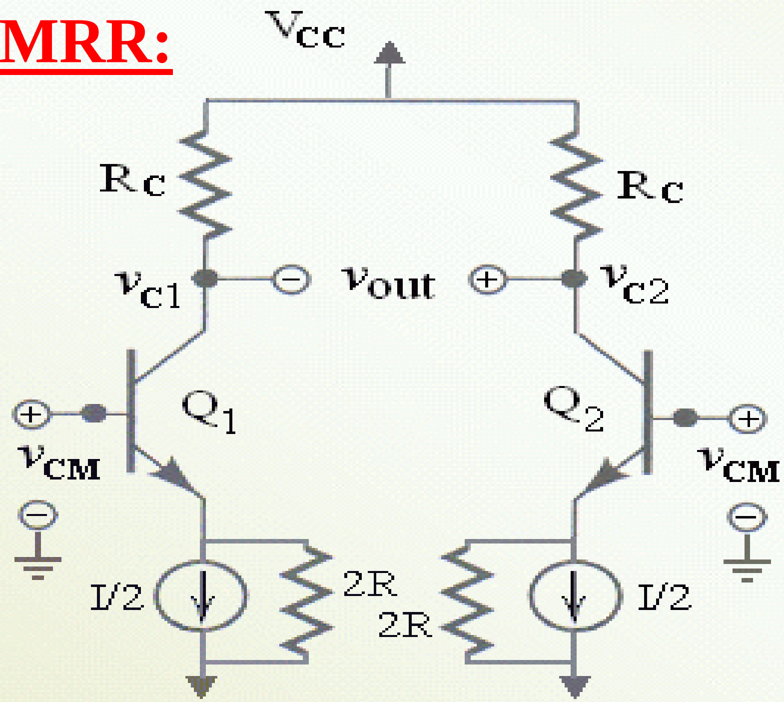
but since, $i_b = \dfrac{i_e}{(\beta+1)}$

input resistance of the DA with R_E is;

$$R_{id} \equiv \frac{v_d}{i_b} = 2(\beta+1)(r_e+R_E)$$

Also, $v_{c1,2} = \pm(\alpha v_d R_C)/2(r_e+R_E)$ ==> Thus, the differential gain, when output is taken differentially is given by; $A_{d\,R_E} = -(\alpha R_C)/(r_e+R_E)$

CMRR:



- The differential amplifier shown has an incremental output resistance 'R' & is fed by a common-mode signal (v_{CM})
- Due to symmetry, the equivalent CM half circuits can be drawn as, where,

$$v_{c1} = v_{c2} = -v_{CM}\frac{\alpha R_C}{2R + r_e} \approx -v_{CM}\frac{\alpha R_C}{2R}$$

- Thus, if output is taken differentially, the common-mode-gain,

$$A_{CM} = (v_{C1} - v_{C2})/v_{CM} = (v_{out})/v_{CM} = 0$$

- But for single ended case, $A_{CM} = \frac{-\alpha R_C}{2R}$

- As practical circuits are never perfectly symmetric, it results in a non-zero common-mode gain (A_{CM}). Thus for, $v_{c1} = -\{v_{CM} \cdot \alpha \cdot R_C\}/(2R + r_e)$ and $v_{c2} = -\{v_{CM} \cdot \alpha \cdot (R_C + \Delta R)\}/(2R + r_e) \rightarrow$ CM gain, $A_{CM} = -\{\alpha \cdot \Delta R\}/(2R + r_e)$

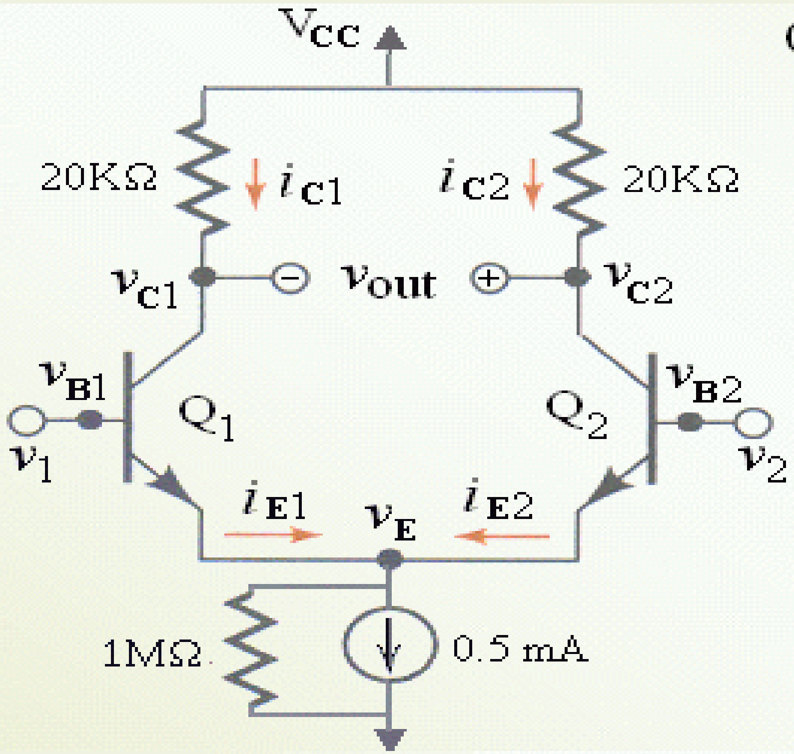
The common-mode-rejection-ratio (CMRR) is a figure of merit for a DA, which express its rejection ratio of unwanted common mode signals (v_{CM}) over input signal of interest (v_d). Thus, $CMRR = \left|\frac{A_d}{A_{CM}}\right| \Rightarrow \left|\frac{\text{differential gain}}{\text{common mode gain}}\right|$

If outputs are taken differentially, using the expression for A_d and A_{CM} we have, $CMRR \rightarrow \infty$ for symmetrical circuit, which resembles an ideal behavior.

But if outputs are taken single endedly, expression of related A_d and A_{CM} gives;

$$CMRR = \{-(g_m \cdot R_C)/(2)\}/\{-(\alpha \cdot R_C)/(2R)\}$$
$$= (g_m \cdot R)/(\alpha)$$

Example Problem:



Q. For given differential amplifier circuit with β=200, ignore 'r_0' effects and find;

(a) The differential gain to a single-ended output *(use any output port)*.

(b) The differential gain when outputs are taken differentially.

(c) The differential input resistance.

(d) The common-mode gain to a single-ended output.

(e) The common-mode gain to a differential output.

Solution:

(a) $r_e = \frac{V_T}{I_E} = 100\Omega$ and $\alpha = \frac{\beta}{\beta+1} = 0.995$, $A_{ds} = -\frac{\alpha R_C}{2r_e} = -\frac{0.995\times 20K\Omega}{2\times 100\Omega} = 99.5\frac{V}{V}$

(b): From previous derivation; $A_d = -\frac{\alpha R_C}{r_e} = -\frac{0.995\times 20K\Omega}{100\Omega} = -199\frac{V}{V}$

(c): The input resistance of DA; $R_{id} \equiv \frac{v_d}{i_b} = (\beta+1)(2r_e) = 40.2\,K\Omega$

(d): For single-ended case; $A_{CM} = \frac{-\alpha R_C}{2R} = \frac{-0.995\times 20K\Omega}{2\times 1M\Omega} = -0.00995\frac{V}{V}$

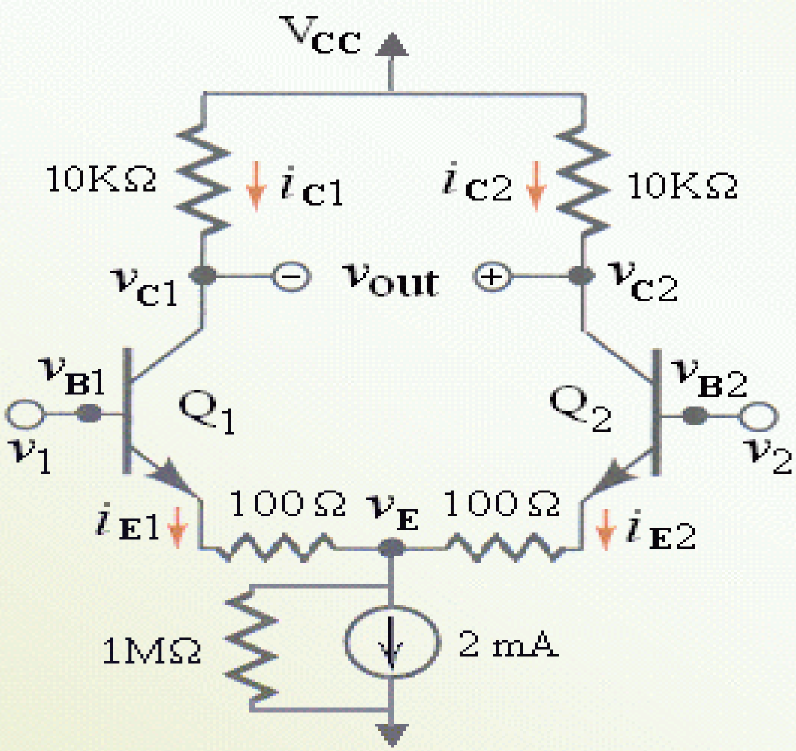
(e): For common-mode gain, $A_{CM} = 0$ as, $v_{C1} = v_{C2}$ resulting $v_{out} = 0$

NOTE

- In differential input case, the two BJT's are supplying ie of different phase (as +vd/2 and –vd/2) and canceling at Emitter point. So no need to consider the REE ➔ Ad

  (this is also shown with current flow, iCs')
- But in CM case, the two BJT's are supplying ie of same phase (as +vCM and +vCM) and flowing via Emitter point. So need to consider the REE ➔ ACM

Exercise Problem: *Solve exercises 7.7, 7.8 and the related Problems of the ch. 7*



Q. For given differential amplifier circuit with β=100, ignore the effects of 'r_0' and 'r_μ' to find the following;

(a) The differential gain to a single -ended output. → Equation not shown in notes

(b) The differential gain when outputs are taken differentially.

(c) The differential input resistance.

(d) If single-ended common-mode voltage gain is -0.005 V/V, find the dB value of common-mode rejection ratio (CMRR). Use A_{ds}

Answers: (a) -39.6 V/V, (b) -79.2 V/V, (c) 25KΩ, (d) 79.9 dB

7.1: The MOS Differential Pair: ➔ *see figure in book page 688*

- MOS DP consist of to matched transistors, similar to BJT DP discussed before
- For same input gate voltages (v_{CM}=0), drain currents are $i_{D1} = i_{D2} \approx I/2$.
- For known V_T , v_{GS} can be calculated from the related i_D equation (in Triode)
- *Solve exercise 7.1: (a), (b), (c) and submit the solution next class.*