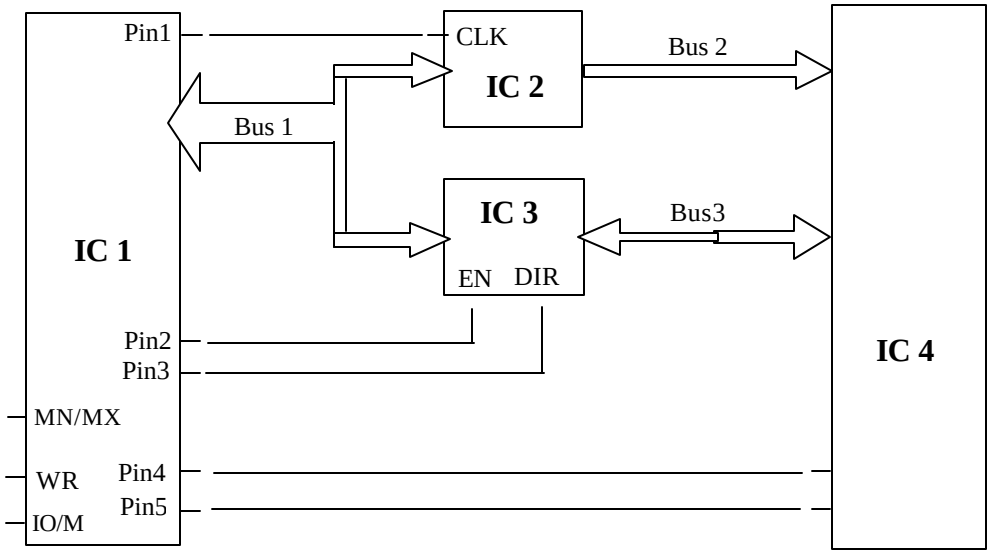
Home work ***Dr. S. Iqbal***

1. The pin connections the 8088 MPU in Min mode (IC1), address bus latch (IC2), data bus transceiver buffer (IC3) and the memory system (IC4) is given in the following figure. For a memory **read** bus cycle, **label** and **name** the required **pins** and **buses**.



(a) Write the name and the Logic-levels of the following pins for above operation;

Pin 1:_____ ; Bus 3:_____ ;

Pin 4:_____ ; Pin 5:_____ ;

Pin 2:_____ ; Pin 3:_____ ;

(b) Write the steps that are performed by CPU to complete the above operation;

_____

_____

_____

_____

_____

_____

2. Fill the following questions:

(i) 8086 microprocessor has _____ bit address-bus and _____ bit data-bus.

(ii) In 8086, the bus cycle consist of at least _____ clock pulses and if required wait status can be inserted by using the _____ pin of the microprocessor.

3. Define the following functions according to the preceding order (*to occure in 1st, 2nd and 3rd*) during a **write** bus cycly **: DEN, IO/M** and **ALE.**

	Signal name	Function
1st to occure		
2nd to occure		
3rd to occure		

4. Solve the problems of Chapter 8.