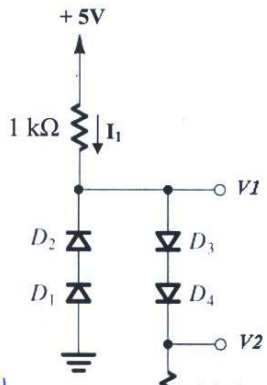
Problem 1

Part (A) [10 points]

For the circuit shown below find the values of the labeled currents and voltages (I_1, V_1, V_2) using the constant voltage model for all diodes (V_{DO}=0.65V).



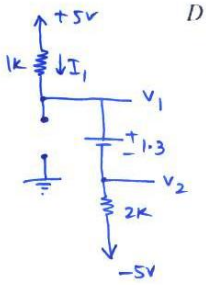
By inspection: D_1 & D_2 OFF

D_3 & D_4 ON

$$I_1 = \frac{5 - 1.3 - (-5)}{3k} = 2.9\,mA$$

$$V_1 = 5 - 2.9m(1k) = 2.1\,V$$

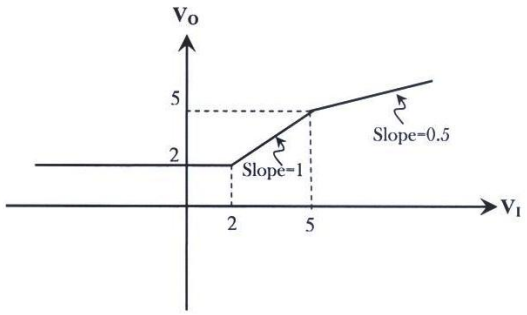
$$V_2 = 2k(2.9m) - 5 = 0.8\,V$$



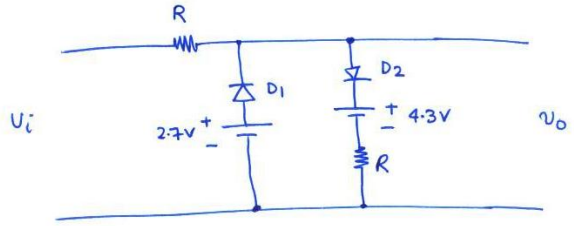
Part (B) [10 points]

Design a limiter circuit using only two diodes, two batteries and a few resistors to provide the transfer function shown below. Assume that the diodes have a 0.7V drop when they conduct.

Specify the value of each component.



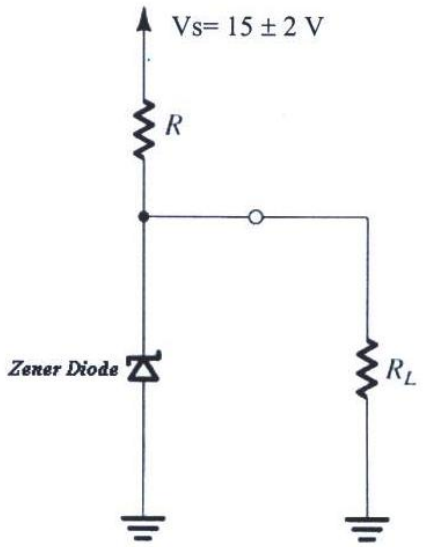
One possible solution is as shown.



Problem 2 [5+5+5+5 points]

The Zener diode in the circuit shown below is specified to have $V_Z = 8V$ at $I_Z = 4$ mA, $r_Z = 25\Omega$, and $I_{Zmin} = 0.5$ mA. The supply voltage V_S is nominally 15 V but can vary by ±2 V. The load resistor R_L is in the range of 4 kΩ to 6 kΩ.

a) Find V_{ZO} for this Zener diode.
b) Find the maximum allowed R that will maintain the circuit to operate as a regulator.
c) Find the change in V_O resulting from the ±2V change in V_S.
d) Evaluate this regulator. (*Hint*: a good regulator has a load regulation less than 30 mV/mA and a line regulation less than 20 mV/V).



a) From the test data and using $V_z = V_{z0} + r_z I_z$

$\Rightarrow V_{z0} = V_z - r_z I_z$

$= 8 - 25(4m)$

$= 7.9$ V

b) Using the formula $R_{max} = \dfrac{V_{smin} - (V_{z0} + r_z I_{zmin})}{I_{zmin} + I_{Lmax}}$

$= \dfrac{13 - (7.9 + 25(0.5m))}{0.5m + 7.9/4K}$

$\approx 2K$

c) $\Delta V_o = \Delta V_s \dfrac{r_z}{r_z + R}$

$= \pm 24.7$ mV

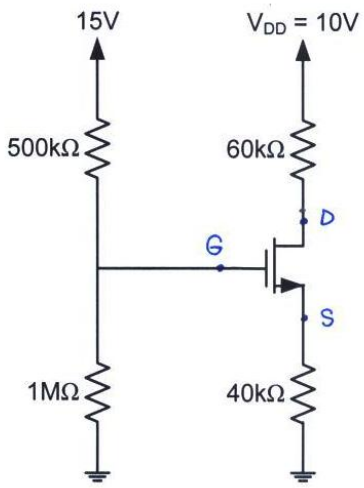
d) LIR = $r_z/(R+r_z)$ = 12.3 mV/V (below standard : good)

LOR = $r_z \| R$ = 24.7 mV/mA (below standard : good)

Problem 3 [3+12+5 points]

The NMOS transistor in the given circuit has $V_t = 1$ V, and $K_n = 25\ \mu A/V^2$ ($K_n = \mu_n C_{ox} W/L$).

a) Find the gate voltage V_G.
b) Find the following: drain and source voltages V_D and V_S; drain and source currents I_D and I_S. Neglect the channel-length modulation effect (*i.e.* assume $\lambda=0$).
c) Explain the phenomenon *channel-length modulation*; illustrate your answer with a sketch of the cross-section of the NMOS.



a) Voltage divider $\Rightarrow$ $V_G = 10V$

b) $V_S = 40K\, I_D$

$V_D = 10 - 60K\, I_D \Rightarrow V_{DS} = 10 - 100K\, I_{DS}$

Assume Saturation

$I_D = K(V_{GS} - V_t)^2$

$I_D = \frac{25\mu}{2}(10 - 40K\, I_D - 1)^2$

Solving the quadratic equation

$\Rightarrow I_D = 0.14\,mA \Rightarrow V_D = 1.53V$

Check assumption:

$V_D < V_G - V_t$

↑

not Saturation.

Assume Triode

$I_D = K[2(V_{GS} - V_t)V_{DS} - V_{DS}^2]$

$= \frac{25\mu}{2}(10 - 100K I_D)[2(9 - 40K I_D) - (10 - 100K I_D)]$

$\Rightarrow 25K I_D^2 + 8.5 I_D - 1m = 0$

solve for I_D

$I_D = -0.432\,mA$ (rejected)

$I_D = 0.092\,mA$

$I_S = 0.092\,mA$

$V_S = 3.7V$

$V_D = 4.48V$

$V_{DS} = 0.78V$

check assumption

$V_D < V_G - V_t$

$0.78 < 10 - 1$ ✓ OK