King Fahd University of Petroleum & Minerals
Electrical Engineering Department
Winter 2012 (112)

EE 203 – Final Exam
Tuesday, May 22, 2012
7:30-10:30 AM

Name					
ID					
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Section	3 and 6	5	1, 4 and 8	7	2

Problem		**Grade**
Part A (28 points)		
Part B (42 points)	Problem 1 (14 points)	
	Problem 2 (14 points)	
	Problem 3 (14 points)	
Total (70 points)		

Note: <u>Part 1 is made of multiple choices questions, only one answer is correct. Clearly fill the box beside the right answer (■). Unclear or multiple answers will be considered as wrong.</u>

Part A: Multiple Choices Questions **[2 points each]**

In each of the questions below, clearly fill the box beside the correct answer.

Question 1:

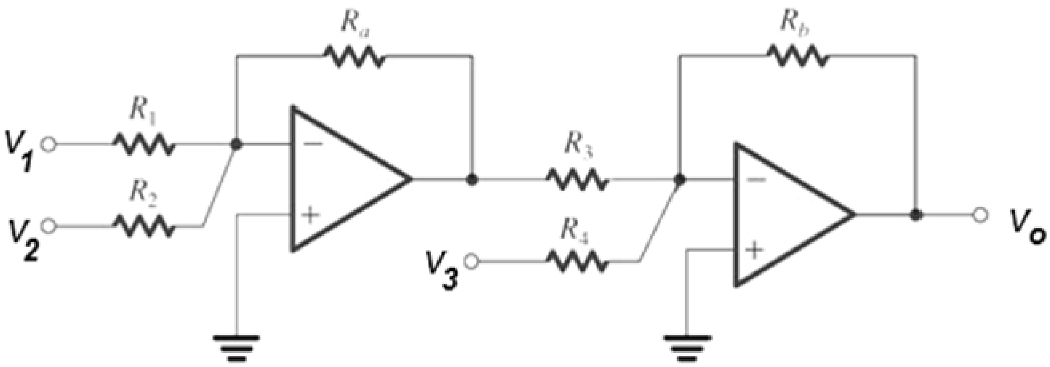
For the OPAMP circuit shown below, where $R_1 = 2\ k\Omega$, $R_2 = R_3 = R_4 = 1\ k\Omega$ and $R_a = 2\ k\Omega$ and $R_b = 3\ k\Omega$. The output voltage V_o is given by:

☐ $V_o = 3V_1 + 6V_2 - 3V_3$.

☐ $V_o = 6V_1 - 6V_2 - 3V_3$.

☐ $V_o = 3V_1 + 6V_2 + 3V_3$.

☐ $V_o = 3V_1 - 6V_2 + 3V_3$.



Question 2:

The voltage drop across a reverse biased diode is about:

☐ 0.0 V

☐ 0.2 V

☐ 0.7 V

☐ unknown

Question 3:

In a forward biased pn junction:

☐ The electrons flow from the p side to the n side.

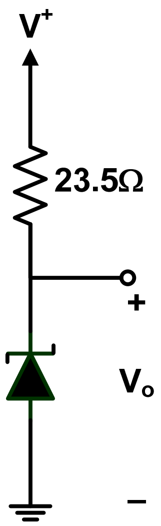
☐ The electrons flow from the n side to the p side.

☐ The electrons remain in the n region.

☐ The electrons remain in the p region.

Question 4:

The voltage regulator shown in the figure below, uses a Zener diode having a resistance r_z=2Ω, Find the change in the output voltage (V_o) when the input voltage (V^+) changes by 1.3V.



☐ $\Delta V_o = 1.2$ mV

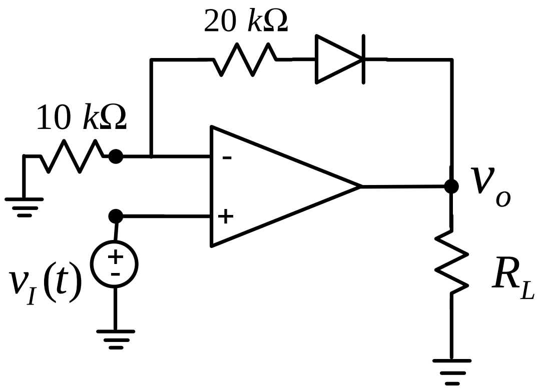
☐ $\Delta V_o = 102$ mV

☐ $\Delta V_o = 65$ mV

☐ $\Delta V_o = 110$ mV

Question 5:

The circuit shown in the figure below has an ideal opamp and an ideal diode. If a sinusoidal input voltage source is applied, the circuit will work as:



☐ Half wave rectifier.

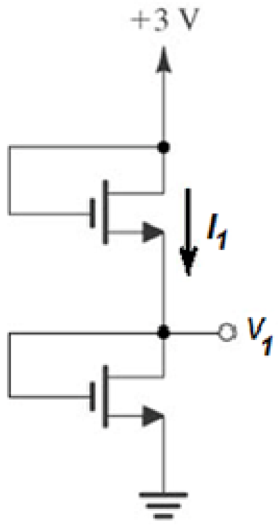
☐ Full wave rectifier.

☐ Inverting amplifier.

☐ Difference amplifier.

Question 6:

For the MOS circuit shown below, the two transistors are identical and have the following parameters: $V_t = 1\text{V}$, $k_n' \frac{W}{L} = 2\ \text{mA/V}^2$, and $\lambda = 0$. The voltage V_1 and the current I_1 are:



☐ $V_1 = 1.5\ \text{V}$ and $I_1 = 250\ \mu\text{A}$.

☐ $V_1 = 1.2\ \text{V}$ and $I_1 = 40\ \mu\text{A}$.

☐ $V_1 = 3\ \text{V}$ and $I_1 = 0\ \mu\text{A}$.

☐ $V_1 = -1.5\ \text{V}$ and $I_1 = 200\ \mu\text{A}$.

Question 7:

The MOSFET can be used as a constant current source when it operates in:

☐ The pinch-off (saturation) region.

☐ The linear region.

☐ The triode region.

☐ The cut-off region.

Question 8:

The phase shift between the input and output signals in common-emitter amplifiers is:

☐ 0° .

☐ 90° .

☐ 180° .

☐ 270° .

Question 9:

A receiver requires an output amplifier stage having high input resistance and low output resistance. Which of the following amplifier configurations can be used?

☐ Common source amplifier.

☐ Common source amplifier with R_s.

☐ Common gate amplifier.

☐ Common drain amplifier.

Question 10:

The BJT can be used as an amplifier if:

☐ The EB junction is reverse biased and CB junction is forward biased.

☐ The EB junction is forward biased and CB junction is reverse biased.

☐ The EB junction is forward biased and CB junction is forward biased.

☐ The EB junction is reverse biased and CB junction is reverse biased.

Question 11:

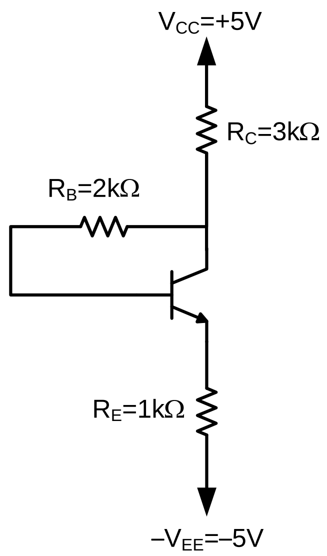
For the circuit shown in the figure below, V_{BE}=0.7V, the transistor is in the active mode and has β=50.
The emitter current I_E is given by:

☐ $I_E = 2.5$ mA

☐ $I_E = 2.65$ mA

☐ $I_E = 2.30$ mA

☐ $I_E = 2.33$ mA



Question 12:

MOSFET in digital circuits mostly work in:

☐ Triode and pinch off (saturation) region.

☐ Triode and cut off region.

☐ Cut off and pinch off (saturation) region.

☐ Active and pinch off (saturation) region.

Question 13:

In CMOS logic circuits, V_{IL} is defined as:

☐ The maximum input voltage that can be considered as high input.

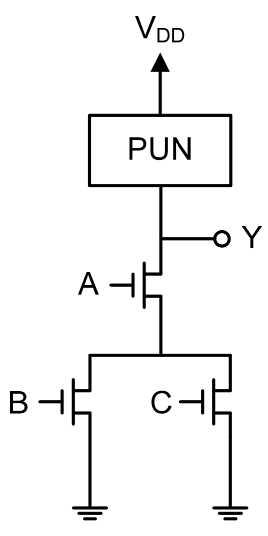
☐ The minimum input voltage that can be considered as low input.

☐ The maximum input voltage that can be considered as low input.

☐ The minimum input voltage that can be considered as high input.

Question 14:

For the circuit shown in the figure below, the output Y is given by:



☐ $Y = A \cdot (B + C)$

☐ $Y = \overline{A} \cdot (\overline{B} + \overline{C})$

☐ $Y = \overline{A} + (\overline{B} \cdot \overline{C})$

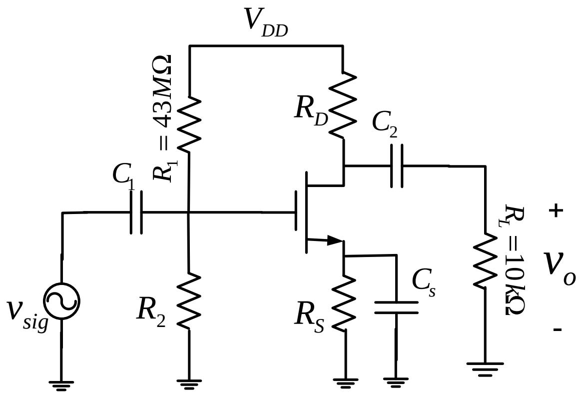
☐ $\overline{Y} = \overline{A} \cdot (\overline{B} + \overline{C})$

Part B: Problems

Problem 1: [14points]

Given a MOSFET with the following parameters, $V_t = 2\text{V}$, $k_n' \dfrac{W}{L} = 5\ \text{mA/V}^2$, and $\lambda = 0$ (no channel length modulation effect), the available DC voltage source is $V_{DD} = 15\text{V}$. It is required to design the common source amplifier shown in the figure below. The biasing point is set to $V_{DS} = \dfrac{V_{DD}}{2}$ and $I_D = 2.5\ \text{mA}$. The amplifier also must provide a voltage gain $\dfrac{v_o}{v_{sig}} = -10\ \text{V/V}$.

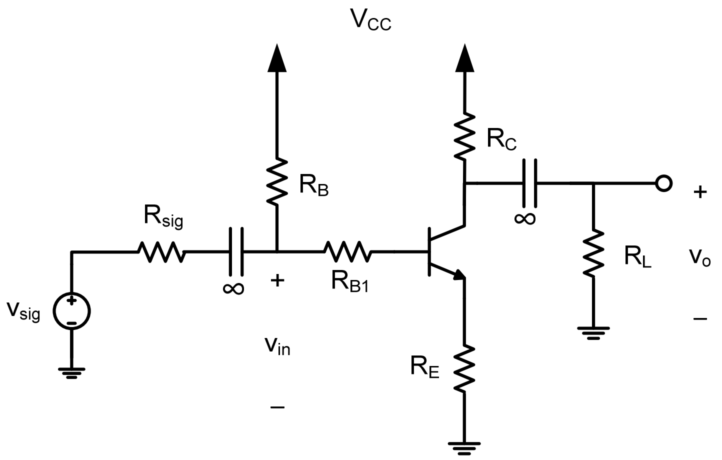
Find the values of the resistors R_D, R_s and R_2.



Problem 2: **[14 points]**

The transistor in the circuit below is biased in the active region and has V_{BE}=0.7V, and β=100. Neglect the effect of Early voltage.

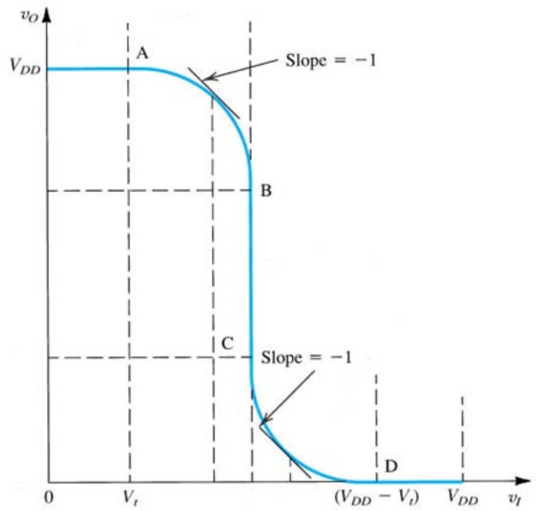
1. Calculate the value of the input resistance R_{in}.
2. Calculate the value of the output resistance R_{out}.
3. What is the value of the gain (v_o/v_{sig})?
4. Suggest a way to increase the gain (no need for calculations).



<u>Problem 3:</u> [14 points]

<u>Problem 3 - A:</u> [6 points]

1. Which logic gate has the voltage transfer characteristic shown below?
2. Clearly label V_{OL}, V_{OH}, V_{IL}, and V_{IH} in the figure.
3. Express the noise magins as a function of the voltages V_{OL}, V_{OH}, V_{IL}, and V_{IH}?



Problem 3 - B: [6 points]

1. Sketch the complete CMOS logic circuit using **minimum number of transistors** that realize the function below. (Assume that the available inputs are A, B and C).

   $Y = \overline{\overline{B} + A \cdot C}$

2. What is total number of transistors needed?
3. Find the transistor sizing for the circuit of question 1 in terms of the size of the inverter's transistors.

Problem 3 – C: [2 points]

1. Draw the **complete circuit (transistors)** using pass transistor logic (transmission gate) to realize the following function:

   $M = CA + \overline{C}B$