King Fahd University of Petroleum & Minerals
Electrical Engineering Department
EE203: Electronics I (111)

| Instructor Information | Dr. Oualid Hammi | Office 59-0012-5 | Phone: 7394 | Email: ohammi@kfupm.edu.sa | Office Hours SMW: 9:00AM to 9:50AM or by appointment |
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| Course Information | Text | Grading | | | | Attendance |
|---|---|---|---|---|---|---|
| | Microelectronic Circuits 5th ed Sedra & Smith | Quizzes + HW + Project 20% | Two Exams 15%+15% | Lab 20% | Final Exam 30% | 6 unexcused absences → Warning<br>9 unexcused absences → DN |

| Week | | Topics to cover | Ch | Sec | Lab Activity |
|---|---|---|---|---|---|
| 1 | Sep. 10 – 14 | Diodes: Introduction – Ideal diode – PN junction – Terminal characteristics of the diode – Physical operation of the diode. | 3 | 1, 2, 7 | No Lab |
| 2 | Sep 17 – 21 | Graphical and analytical diode circuits analysis – Diode Models – The Zener diode. | 3 | 3.1-3.3, 3.5, 3.6, 4.1, 4.2 | Exp 1: Lab Equipment |
| 3 | Sep 24 – 28 | Diode applications: Half and Full-wave rectifiers – Limiting and Clamping circuits and Voltage doublers.<br>Field-Effect Transistors (FETs): Device structure and operation. | 3<br>4 | 5.1-5.4, 6<br>1.1-1.5 | No Lab |
| 4 | Oct 1 – 5 | PMOS structure and operation – CMOS structure – Current-Voltage Characteristic – Role of substrate – MOSFET circuits at DC. | 4 | 1.6-1.8, 2.1-2.5, 3 | Exp 2: PSPICE |
| 5 | Oct 8 – 12 | The MOSFET as amplifier – Biasing – Small signal operation and models – Review. | 4 | 4-6 | Exp 3: Diode Applications |
| **Major Exam 1: Saturday October 15, 2011 (6:00PM – 8:00PM). (Location: B59/R2002 for section 3 and B59/R2003 for section 4.)** | | | | | |
| 6 | Oct 15 – 19 | Single stage amplifier (CS, CG & CD). | 4 | 7 | Exp 4: DC Power Supply |
| 7 | Oct 22 – 26 | Bipolar Junction Transistors (BJTs): Structure and operation – Types – Symbols and conventions – Transistors current-voltage characteristics. | 5 | 1.1-1.3, 1.5, 1.6, 2, 3 | Exp 5: MOSFET Amplifiers |
| 8 | Oct 29 – 31 | BJT circuits at DC – Biasing. | 5 | 4-5 | No Lab |
| **Id al-Adha Vacation: November 1st – November 12th , 2011** | | | | | |
| 9 | Nov. 12 – 16 | Small signal models and analysis – Single stage amplifier (CE). | 5 | 6,7.1-7.4 | No Lab |
| 10 | Nov. 19 – 23 | Single stage amplifier (CB, CC). | 5 | 7.5,7.7 | Exp 6: BJT Characteristics |
| 11 | Nov. 26 – 30 | Differential Amplifiers: MOS BJT Differential amplifiers.<br>Review. | 7 | 1,2,3 | Exp 7: BJT CE Amplifiers |
| **Major Exam 2: Wednesday November 30, 2011 (6:00PM – 8:00PM). (Location: B59/R2002 for section 3 and B59/R2003 for section 4.)** | | | | | |
| 12 | Dec. 3 – 7 | Digital Circuit design overview – The CMOS inverter – CMOS. | 10 | 1.1, 1.2, 2.1, 2.2, | Exp 8: Differential Amp. |
| 13 | Dec. 10 – 14 | Logic circuits – CMOS transistor sizing – Pass transistor logic circuits (PTL) – Basic concept of dynamic logic circuits. | 10 | 3.1-3.8, 4.1, 4.2, 5,6.1 | Exp 9: CMOS Inverter |
| 14 | Dec. 17 – 21 | BJT as a switch – The basic BJT inverter.<br>RTL circuits – Maximum fan-out calculation – ECL logic circuits. | 5<br>11 | 3.4, 10<br>7.1, 7.3, 7.4, 7.7 | Exp 10: BJT Logic Gates |
| 15 | Dec. 24 – 28 | TTL Basic Inverters and NAND gate – BJT vs. MOS Logic: advantage/disadvantages. | 11 | Handout | Lab Final |
| 16 | Dec. 31 – Jan 2 | Review | | | |

**Final Exam: Monday January 16, 2012 @ 7:00PM (6:00PM – 8:00PM). (Location to be specified by the Office of the University Registrar.)**