

King Fahd University of Petroleum & Minerals
Electrical Engineering Department
EE203: Electronics I (102)

Instructor Information	Dr. Oualid Hammi	Office 59/0012-5	Phone: 7394	Email: ohammi@kfupm.edu.sa	Office Hours SMW: 9:30AM to 10:30AM or by appointment
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Course Information	Text Microelectronic Circuits 5 th ed Sedra & Smith	Grading				Attendance
		Quizzes + HW + Project 20%	Two Exams 30%	Lab 20%	Final Exam 30%	6 unexcused absences → Warning 9 unexcused absences → DN

Week	Topics to cover		Ch	Sec	Lab Activity
1	Feb 12 – 16	Diodes: Introduction, Ideal diode, PN junction, Terminal characteristics of the diode, Physical operation of the diode.	3	1, 2, 7	No Lab
2	Feb 19 - 23	Graphical and analytical diode circuits analysis, Diode Models, the Zener diode.	3	3.1-3.3, 3.5, 3.6, 4.1, 4.2	Exp 1: Lab Equipment
3	Feb26 -March 2	Diode applications: half and Full-wave rectifiers, Limiting and Clamping circuits and voltage doublers. Field-Effect Transistors (FETs): Device structure and operation.	3	5.1-5.4, 6	Exp 2: PSPICE
			4	1.1-1.5	
4	March 5 - 9	PMOS structure and operation, CMOS structure, Current –Voltage Characteristic, Role of substrate, MOSFET Circuits at DC.	4	1.6-1.8, 2.1-2.5, 3	Exp 3: Diode Applications
5	March 12 – 16	The MOSFET as amplifier, Biasing, small signal operation and models, Single stage amplifier (CS, CG and CD).	4	4-7	No Lab

Exam 1 Saturday March 19 (6:00-8:00 pm). Exam location: Building 59 room 2001 for section 1 and room 2002 for section 2.

6	March 19 – 23	Single stage amplifier (Continued) (CS, CG & CD).	4	7	Exp 4: DC Power Supply
7	March 26 - April 30	Bipolar Junction Transistors (BJTs): structure and operation, types, symbols and conventions, transistors current-voltage characteristics.	5	1.1-1.3, 1.5, 1.6, 2, 3	Exp 5: MOSFET Amplifiers
8	April 2 – 6	BJT circuits at DC, Biasing, Small signal models and analysis.	5	4-6	Exp 6: BJT Characteristics

Midterm Vacation April 9-13

9	April 16 – 20	Single stage amplifier (CE, and CB).	5	7.1-7.5	No Lab
10	April 23 – 27	Single stage amplifier (CC). Differential Amplifiers: MOS.	5	7.6,7.7	Exp 7: BJT CE Amplifiers
			7	1,2	
11	April 30 – May 4	BJT Differential amplifiers. Digital Circuit design overview, the CMOS inverter.	7	3	No Lab
			10	1.1, 1.2, 2.1, 2.2	

Exam 2 Wednesday May 4 (6:00-8:00 pm). Exam location: Building 22 room 119 for both sections.

12	May 7-11	CMOS Logic circuits, CMOS transistor sizing.	10	3.1-3.8	Exp 8: Differential Amp.
13	May 14-18	Pass transistor logic circuits (PTL), Basic concept of dynamic logic circuits. BJT as a switch, The basic BJT inverter.	10	4.1, 4.2, 5,6.1	Exp 9: CMOS Inverter
			5	3.4, 10	
14	May 21-25	RTL circuits, maximum fan-out calculation, ECL logic circuits.	11	7.1, 7.3, 7.4, 7.7	Exp 10: BJT Logic Gates
15	May 28 - June 1	TTL Basic Inverters and NAND gate, BJT vs. MOS Logic: advantage/disadvantages.	11	Handout	Lab Final

Final Exam Sunday June 12, 2011 @ 7:00PM