King Fahd University of Petroleum and Minerals

Electrical Engineering Department

EE200: Digital Logic Circuit Design
First Semester 2010-2011 (101)

A. Course Information

Text Book:	**Digital Design (4th Edition) by M. M. Mano**			
Course	Name	Office	Phone	Sections
Coordinator:	Dr. Mohammad S. Sharawi, *msharawi@kfupm.edu.sa*	59/1091	4810	
Instructors:	Your Section Instructor is: **Dr. Mahmoud M. Dawoud ,** *mmdawoud@kfupm.edu.sa* Office Hours: 8:00 am– 8:50 am, SMW Or by appointment	59/2070	2299	01 and 03
Lab	Name	Office	Phone	Sections
Coordinator:	Dr. Essam Hassan, *ehassan@kfupm.edu.sa*	59-2100	2370	
Grading:	Assignments and Quizzes	Laboratory	Design Project	Two Majors	Final
	15%	20%	5%	30%	30%
	First Major	**Second Major**	**Lab Final**	**Final**
Exams Dates:	**Mon. October 25, 2010**	**Mon. December 13, 2010**	**January 8- 12, 2011** Your Lab time In your Lab	Per the schedule from the registrar's office
Exams Times:	7 – 9 PM	7 – 9 PM		
Exams Places:	To be announced	To be announced		
Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade	Last day to drop all courses with "WP/WF" Thru Registrar's office.
	October 6, 2010	November 3, 2010	January 9, 2011

Note #1: Final Exam is **coordinated** and **comprehensive** (i.e. it is common for all sections and covers chapter 1-7 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during the normal Lab session. **Major Exams are also coordinated**.

Note #2: According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's grade.

Note #3: It is your responsibility to solve the ***practice problems*** as soon as the material is covered in the class. Solution will be posted on **WebCT(**http://ocw.kfupm.edu.sa/**)**.The ***practice problems*** set will not be collected.

Note #4: Your instructor will give you other home work assignments which will be collected and graded. Quizzes will be given regularly based on the homework and the ***practice problems***..

Note #5: **A** design project will be assigned around week 10 and will be due at the end of week 14**.**

Note #6: Class notes, announcements and HW solutions will be posted on the class webpage at: http://faculty.kfupm.edu.sa/EE/mmdawoud/
it is your responsibility to check announcements regularly.

B. Course Details.

1. **Course (Catalog) Description**

   Number systems & codes. Logic gates. Boolean Algebra. Karnaugh maps. Analysis and synthesis of combinational systems, decoders, multiplexers, adders and subtractors, PLA's. Types of flip-flops. Memory concept. Registers. Introduction to sequential circuit design.

2. **Prerequisites(s)**

   Calculus I (MATH 101)
   General Physics I (PHYS 101)

3. **Course objectives** are to

   1. Introduce the students to the the digital principles with emphasis on logic design.
   2. Familiarize the students with the necessary mathematical tools such as number systems, codes, and Boolean algebra.
   3. learn the principles of analysis and design of combinational logic circuits
   4. learn the principles of analysis and design of sequential logic circuits.

4. **Learning Outcomes**

   After successfully completing the course, the students will be able to

   Outcome1: apply knowledge of number systems, codes and Boolean algebra to the analysis and design of digital logic circuits.

   Outcome 2: identify, formulate, and solve engineering problems in the area of digital logic circuit design.

   Outcome 3: use the techniques, skills, and modern engineering tools such as logic works, necessary for engineering practice.

   Outcome 4: to function on multi-disciplinary teams through digital circuit experiments and projects.

   Outcome 5: to design a digital system, components or process to meet desired needs within realistic constraints.

5. **Topics Covered**

   - Binary Numbers, Number Base Conversions,
   - Complements, Signed Binary Numbers, Binary Codes,
   - Binary Logic, Boolean Algebra and digital logic gates,
   - Forms of logic functions and K-map simplification,
   - Analysis and design of combinational logic circuits,
   - Adders, Multipliers, Magnitude Comparator, Decoders, Multiplexers,
   - Programmable logic devices,
   - Flip-flops and sequential circuits,
   - Registers and counters.

6. **References.**

   - *Fundamentals of Digital Logic with Verilog Design*, S. Brown and Z. Vranesic, 2nd Edition, McGraw Hill, 2008.
   - *Logic and Computer Design Fundamentals*, M. Morris Mano and C. R. Kime, 4th Edition, Prentice Hall, 2008.

C. Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	Sep. 25	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab.
2	Oct. 2	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Introduction to Lab. Equipment, Exp#1: Binary & Decimal Numbers
3	Oct. 9	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	No Lab.
4	Oct. 16	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.5	Exp#2: Digital Logic Gates
5	Oct. 23	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function.	3.6-3.9	Exp#3: Introduction to LogicWorks **Exam # 1**
6	Oct. 30	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	4.1-4.4	Exp#4: Boolean Algebra
7	Nov. 6	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#5: Simplification
EID Al-Fitr Break				
8	Nov. 27	Encoders and Multiplexers, Random Access Memory.	4.9-4.11, 7.2, 7.3	Exp#6: Code Conversion
10	Dec. 4	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#7: Adders/Subtractors
11	Dec. 11	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.4	Exp#8: Multiplexers **Exam # 2**
12	Dec. 18	Analysis of Clocked Sequential Circuits, State Reduction and Assignment.	5.5, 5.7	Exp#9: Design with ROM's
13	Dec. 25	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops.	5.8	Exp#10: Flip-flops
14	Jan. 1	Registers and Shift Registers	6.1, 6.2	Exp#11: Counters & Sequential Logic
15	Jan. 8	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	**Lab Final**
16	Jan. 15	Revision.		

D. Practice Problems

Chapter 1: 5,7,9,18,20,29,35
Chapter 2: 2, 8,12,15,18,20
Chapter 3: 2,7,12,15,19,24
Chapter 4: 5,11,13,20,25,29,31,35
Chapter 7: 15,18,19,21,25
Chapter 5: 2,6,9,12,19
Chapter 6: 5,7,8,12,21