A new CMOS tunable floating capacitance multiplier

Munir A. Al-Abesi

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ABSTRACT
This paper presents a new tunable complementary metal oxide semiconductor (CMOS) floating capacitance multiplier. The multiplier uses the translinear principle with metal-oxide semiconductor field effect transistors operating in the sub-threshold region. The multiplication factor is tunable to meet the design requirements. The Tanner T-spice simulator confirms the functionality of the design using 0.18-µm CMOS Technology. The circuit operates from a supply voltage of ±0.75 V and the capacitance can be magnified 300-fold.

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Capacitance multiplier; sub-threshold; translinear loop; low frequency filters; biomedical circuits; oscillators

Introduction
High performance and very low frequency analogue filters are widely used in biomedical applications (Stotts, 1989). In these applications, the frequency of interest is in the sub-hertz to kilohertz region which requires large time constants to design fully integrated filters. A large capacitance and/or resistance are needed to implement such large time constant. However, it is impractical to implement large capacitances and large resistances in integrated circuits. Therefore, capacitance/resistance multipliers are the best approach to achieving large time constants using less chip area.

Over the years, researchers have developed several techniques to implement on-the-chip capacitance and impedance multipliers. There are many approaches reported in the literature for floating C-multiplier (Afzal, 2013; Ahmed, Khan, & Minhaj, 1995; Jaikla, Lahiri, & Siripruchyanum, 2010; Kafe & Psychalinos, 2014; Matsumoto, Fujii, Nishioka, Abe, & Ohbuchi, 2013; Matsumoto, Nishioka, Ohbuchi, Fujii, & Fujiim, 2015). An operational transconductance amplifier (OTA)-based floating-type impedance scaling circuit has been reported (Ahmed et al., 1995). Three OTAs are used in addition to one Op-Amp and one buffer. In Afzal (2013), a digitally programmable floating impedance multiplier is presented. The design is based on differential voltage current conveyors and a digital control module. Another complex design using tunable four-terminal floating Nullors is reported in Jaikla et al. (2010). This design uses the log and antilog circuits in addition to two nonlinear transconductors. The work in Matsumoto et al. (2013) is an OTA-based design with a fixed multiplication factor. Moreover, in Matsumoto et al. (2013), large channel widths of 90 µm are required for 12 transistors. In Kafe & Psychalinos (2014), a floating capacitor emulator with impedance scaling is presented. The design used seven log-domain and Sinh-domain
integrator blocks. This leads to a complex design with large areas on the chip and large power consumption. Recent work presented in Matsumoto et al. (2015) proposed two designs to simulate the floating capacitor. In both designs, a 90-µm channel width is used for most of the transistors. Also, the scaling factor is based on the aspect ratios of the mirrors, which mean that there is a lack of controllability in the scaling factor. A common drawback of these designs (Afzal, 2013; Ahmed et al., 1995; Jaiкла et al., 2010; Kafe & Psychalinos, 2014; Matsumoto et al., 2013, 2015; Stotts, 1989) is the large area on the chip—hence, there is more power consumption and higher cost.

In this paper, we present the design for a new compact controllable floating C-multiplier circuit. In the sections that follow, the proposed design is presented in “Proposed floating C-multiplier” section. The “Simulation Results” section presents the simulation results and the “Conclusion” section draws the conclusion.

Proposed floating C-multiplier

The block diagram of the proposed circuit is shown in Figure 1 where Z is the impedance to be scaled.

With reference to Figure 1, the differential unity gain (DUA) amplifier output is given by the following equations:

\[ V_x = V_1 - V_2 \]  

\[ Z = \frac{V_x}{i_x} = \frac{V_1 - V_2}{i_x} \]  

The equivalent impedance seen between nodes \( V_1 \) and \( V_2 \) is given by the following equation:

\[ Z_{eq} = \frac{V_1 - V_2}{i_1} = \frac{V_1 - V_2}{i_2} = \frac{V_1 - V_2}{i_o} = \frac{V_1 - V_2}{K \times i_x} = \frac{Z}{K} \]  

where \( i_o = K \times i_x \) is the current output, \( i_1 = i_2 = i_o \) and \( K \) is the gain of the amplifier.

The circuit diagram of the proposed C-multiplier is shown in Figure 2. Four identical metal–oxide semiconductor field effect transistor (MOSFET) transistors (M1–M4) biased in the sub-threshold region to form a translinear loop that will act as a current amplifier.

Figure 1. Block diagram of the proposed design.
The input is a regulated cascade to make the node at the drain of M1 low impedance; hence, it can sense the current passing through the capacitor to be scaled. It will also enhance the upper frequency corner in the operational range. The sub-threshold operation offers a large output resistance that enhances the low frequency corner of the operational range.

Transistors M5-M7 form a current mirror to provide copy of the current \(i_o\). The DUA circuit diagram used is shown in Figure 3.

Applying Kirchhoff voltage law to the translinear loop formed by transistors M1–M4 (Figure 2) yields:

\[
V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}
\]  

(4)

Figure 2. Circuit diagram of the proposed C-multiplier.

Figure 3. Differential unity gain amplifier.
For the MOSFET to work in sub-threshold mode, the gate-to-source voltage should be less than the threshold voltage. The drain current of an nMOS operating in subthreshold forward saturation is given by the following equation:

\[ I_D = I_{DO} \frac{W}{L} e^{\left( \frac{V_{GS} - V_{TH}}{nV_T} \right)} \] (5)

where \( I_{DO} \) is the saturation current, \( n \) is the sub-threshold slope factor, \( W \) is the channel width, \( L \) is the channel length of the transistor, \( V_T \) is the thermal voltage, \( V_{TH} \) is the threshold voltage and \( V_{GS} \) is the gate-to-source voltage.

To keep the MOSFETs operating in the sub-threshold forward saturation, the following conditions must be satisfied:

\[ \frac{I_{DO}}{I_D} << 1 \text{ and } V_{DS} > 4V_T \]

Using Equation (5), the gate-to-source voltage is expressed as follows:

\[ V_{GS} = nV_T \ln \left( \frac{I_D}{I_{DO}} \frac{L}{W} \right) + V_{TH} \] (6)

Combining Equations (4) and (6), and assuming all sources are connected to their respective bulk, yields the following:

\[ I_{D3} \times I_{D4} = I_{D1} \times I_{D2} \] (7)

where \( I_{Di} \), \( i = 1, 2, 3, \) and 4 is the drain current of transistor \( M_i \).

With reference to Figure 1, Equation (7) can be rewritten as follows:

\[ (i_o + i_4) \times i_3 = i_2 \times (i_1 + i_x) \] (8)

Or

\[ (i_o + i_4) = K \times (i_1 + i_x) \] (9)

where \( K = \frac{i_2}{i_3} \).

From Equation (9), if \( i_4 = K \times i_1 \) then

\[ i_o = K \times i_x \] (10)

The floating impedance between nodes \( V_1 \) and \( V_2 \) in Figure 1 is given by the following equation:

\[ Z_{eq} = \frac{V_1 - V_2}{i_1} = \frac{V_1 - V_2}{i_2} \] (11)

Assuming that the scaled impedance \( Z \) is much greater than the total impedance at the drain of M1, then the current \( i_x \) passing through \( Z \) is given by the following equation:

\[ i_x = \frac{V_x}{Z} = \frac{V_1 - V_2}{Z} \] (12)

because \( i_1 = i_2 = i_o = K \times i_x \) (13)
Combining Equations (11), (12) and (13), the equivalent impedance is given by the following equation:

$$Z_{eq} = \frac{V_1 - V_2}{K \times i_x} = \frac{Z}{K} \quad (14)$$

If $Z$ is replaced by a capacitor, then

$$Z_{eq} = \frac{1}{sCK} \quad (15)$$

It is clear that Equation (15) realises a tunable floating C-multiplier. The multiplication factor $K$ is controlled by the bias currents $I_2$ and $I_3$. Two circuits are used for biasing, one to produce $I_1$ and $I_3$ and the second one to produce $I_5$, $I_4$ and $I_2$ the value of each is equal to $K / C_2 I_1$.

**Simulation results**

The validity of the proposed circuit was confirmed using Tanner T-spice. The transistor model used in the simulation is a BSIM3V3 0.18 µm process model. The capacitor to be scaled is 10 pF, and the supply voltage is ±0.75 V. The aspect ratios for all transistors used are shown in Table 1. The currents $I_1$ and $I_3$ are set to 1 nA and $I_4 = I_5 = I_2 = K \times I_1$. The bias current for the DUA $I_B = 5 \mu A$. The tuning variable $K$ can be varied from 1 to 300. To check the range of frequency over which the proposed capacitance multiplier can be used, $K$ was set to 20. An ac signal was applied and the current passing through the equivalent impedance was measured to find $Z$. A plot of the capacitor impedance for the simulated and calculated results are shown in Figure 4. It is clear from the plot that the simulated capacitor is in close agreement with the ideal case from 1 mHz to 10 kHz and this is sufficient for biomedical applications.

The performance of the new design is compared with previously published work and is summarised in Table 2.

From Table 2, it is clear that the proposed design is superior to others in terms of controllability, low frequency corner and area on the chip. However, the power consumption is higher than the design reported in Matsumoto et al. (2015) and this is because of the DUA which is biased in strong inversion.

The proposed design was used in the design of an RC high pass filter with $R = 10 \, \text{M}\Omega$, $C = 10 \, \text{pF}$ and the current $I_1 = 2 \, \text{nA}$. A plot of the frequency response for both simulated and calculated results are shown in Figure 5 for different values of $K$ (20, 50, 300) to achieve cutoff frequencies of 79.5, 32, 5 Hz, respectively. It is clear from the plot that the proposed C-multiplier is working properly. However, the deviation between ideal and simulated results will increase as the multiplication factor $K$ increases. This increasing $K$ will lead to higher current in M4 and M7 and hence $r_{oa}$ and $r_{og}$ will decrease. This will affect the equivalent impedance seen between $V_1$ and $V_2$ and lead to change in the cutoff frequency.

The proposed circuit was simulated for the time domain behaviour. The input signal is 260 mV peak-to-peak and 1 kHz frequency which is the cutoff frequency of

<table>
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<th>Table 1. Aspect ratios for all transistors.</th>
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<td>M1–M7</td>
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<td>7 µm/2 µm</td>
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the high pass filter, $R = 10 \, \text{M}\Omega$, $K = 20$ and $C = 10 \, \text{pF}$. The phase of the filter at this frequency is $45^\circ$. The simulation results shown in Figure 6 confirm that the circuit performs well in the time domain. The total harmonic distortion at maximum input is 1.73%.

The input and output ranges are limited by the differential input of the DUA since both terminals are connected to the two inputs of the DUA. Simulation results indicate that the input range is $-130$ to $130 \, \text{mV}$ and the output range can swing to the same level. However, the difference between the input and the output should be less than the input range of the differential amplifier allowed for linear operation.

Temperature simulations were performed on the high pass filter circuit with $I_1 = I_3 = 2 \, \text{nA}$, $C = 10 \, \text{pF}$, $R = 10 \, \text{M}\Omega$ and $K = 20$, 50, 300. The temperature was varied from $-25 \, ^\circ\text{C}$ to $75 \, ^\circ\text{C}$. A plot of the simulation results is shown in Figure 7. It is clear from the plot that the circuits are insensitive to temperature variations.
Monte Carlo analysis using the statistical model provided by the fabrication vendor for 0.18-µm complementary metal oxide semiconductor (CMOS) technology is used to see how the proposed circuit behaves if there is mismatch between the transistor parameters. Running Monte Carlo analysis for 100 iterations and 0.15 standard deviation yields the frequency response curve for the high pass filter using the same parameters. The simulation results depicted in Figure 8 indicate that the design is insensitive to mismatch in transistor parameters.

The proposed C-multiplier was used in the design of an RLC bandpass filter with $L = 1 \, \text{H}$, $R = 2 \, \text{M} \Omega$, basic capacitance is $10 \, \text{pF}$, $I_1 = I_3 = 10 \, \text{nA}$, and $K = 20, 50, 300$. Simulation results shown in Figure 9 confirm that the frequency response of the filter designed using C-multiplier is functioning properly with small deviation in the lower corner form ideal design.

**Figure 5.** Plot of the frequency response of the high pass filter.

**Figure 6.** Plot of the time domain response of the high pass filter.
Conclusion

In this paper, the design of a new floating-type C-multiplier circuit was presented. The proposed circuit is tunable and can increase the capacitance size 300 times. The usefulness of the design is that it can be an essential block in the design of low frequency circuits.
filters for biomedical circuits that require large time constants utilising small area. The design can be modified to implement inductance and resistance multiplier as well.

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Disclosure statement

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References


Figure 9. Plot of the frequency response of the bandpass filter for ideal and simulated capacitor.
