Design and Analysis of Fractional-N Frequency Synthesizers For Wireless Communications

Alaa Hussein

Outline

- Motivation
- Background
- Novel Fractional-N Frequency Synthesizers
- Novel Analog-to-Digital Architecture
- Conclusions

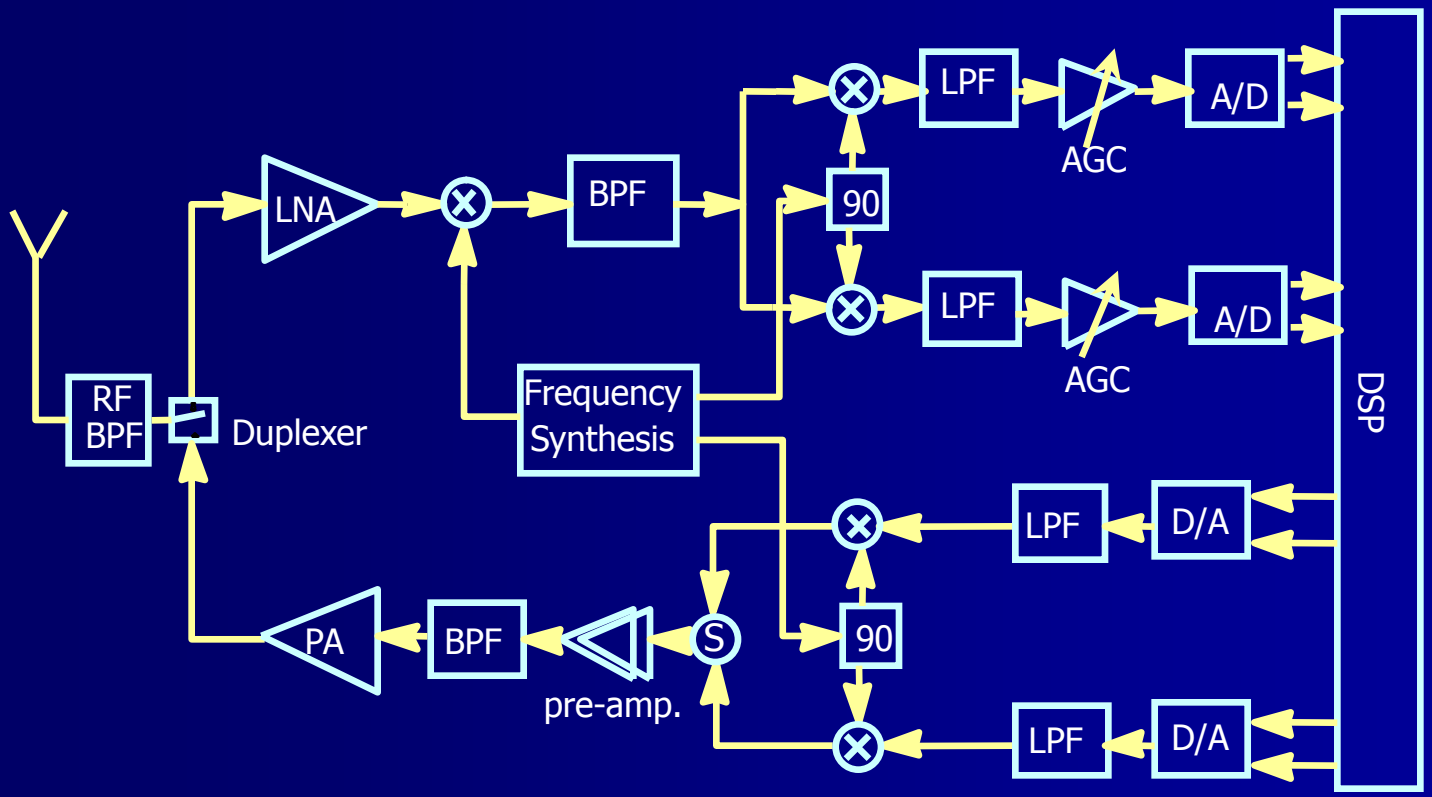
Motivation

- Higher demand for wireless communications and limited bandwidth
  - Frequency synthesizers require tighter performance characteristics (lock time, phase noise, and spurs) to accommodate this increased demand
  - Mobile devices need low-power design

Outline

- Motivation
- Background
- Novel Fractional-N Frequency Synthesizers
- Novel Analog-to-Digital Architecture
- Conclusions

Wireless Transceiver

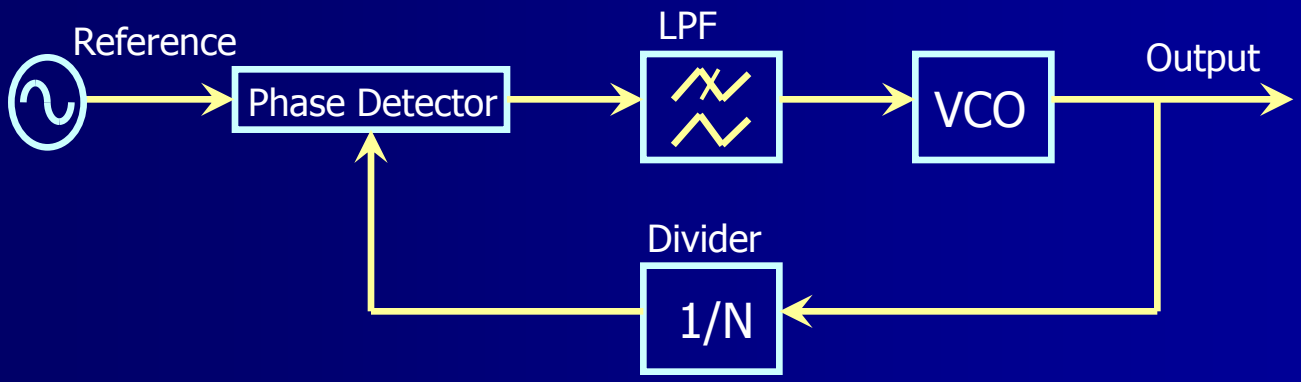


Wireless Frequency Standard

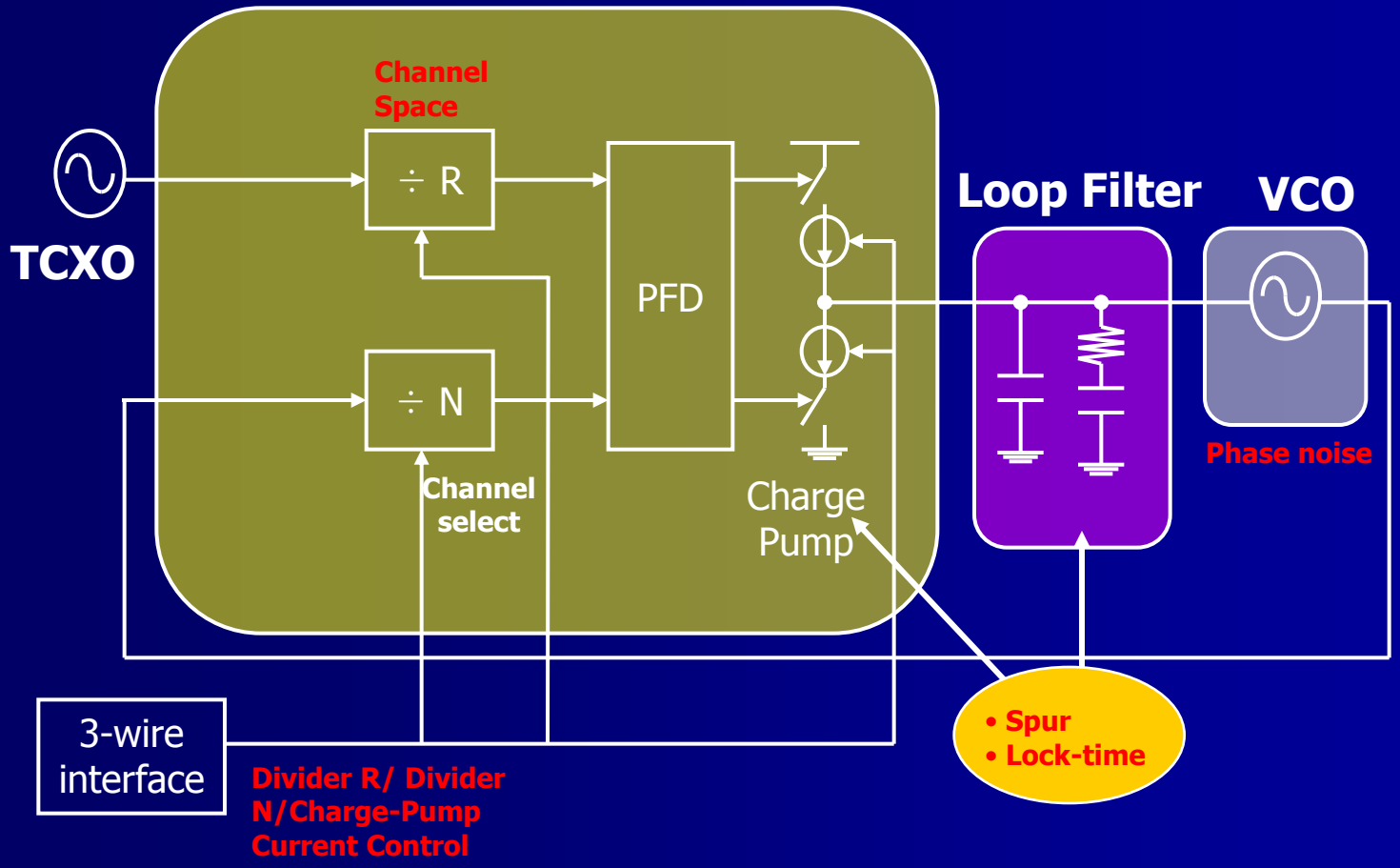
Wireless Standard	Frequency Band (MHz)	Channel Bandwidth	Channel Spacing	Switching Time	F_{vco} (MHz)	F_{vco} / F_{ref} (=N)
AMPS	Rx : 869 ~ 894 Tx : 824 ~ 849	30 kHz	30 kHz	~10 ms	954.39 ~ 979.35	31813 ~ 32645
IS-95	Rx : 869 ~ 894 Tx : 824 ~ 849	1.25 MHz	10 kHz	< 500 μs	954.39 ~ 979.35	161962 ~ 164962
PCS (US)	Rx : 1930 ~ 1990 Tx : 1850 ~ 1910	1.25 MHz	10 kHz	~5 ms	1719.62 ~ 1779.62	171962 ~ 177962
GSM	Rx : 925 ~ 960 Tx : 880 ~ 915	200 kHz	200 kHz	577 μs	1150 ~ 1230	5750 ~ 6150
GPRS	Rx : 925 ~ 960 Tx : 880 ~ 915	200 kHz	200 kHz	200 μs	1150 ~ 1230	5750 ~ 6150
DCS-1800	Rx : 1805 ~ 1880 Tx : 1710 ~ 1785	200 kHz	200 kHz	-	1530 ~ 1610	7650 ~ 8050
DECT	Rx : 1880 ~ 1900 Tx : 1880 ~ 1900	1.728 MHz	-	450 μs	-	-

PLL Synthesizer Basics

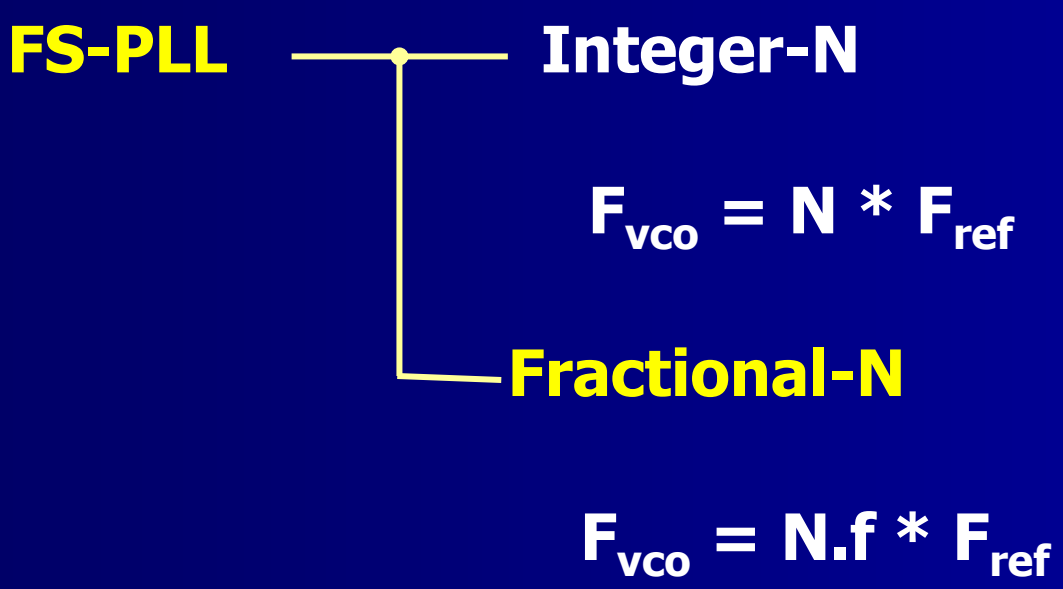
- The phase detector PD compares the reference frequency to the frequency from a feedback divider N
- PD controls the frequency of a voltage controlled oscillator VCO according to the phase/frequency difference of its inputs
- The output of the PD is pulsed and is translated to dc by the action of the loop filter
- The VCO frequency is divided back down to reference frequency by N divider
- By changing the N divider the output frequency can be controlled
- The output frequency resolution equals reference frequency (channel spacing)



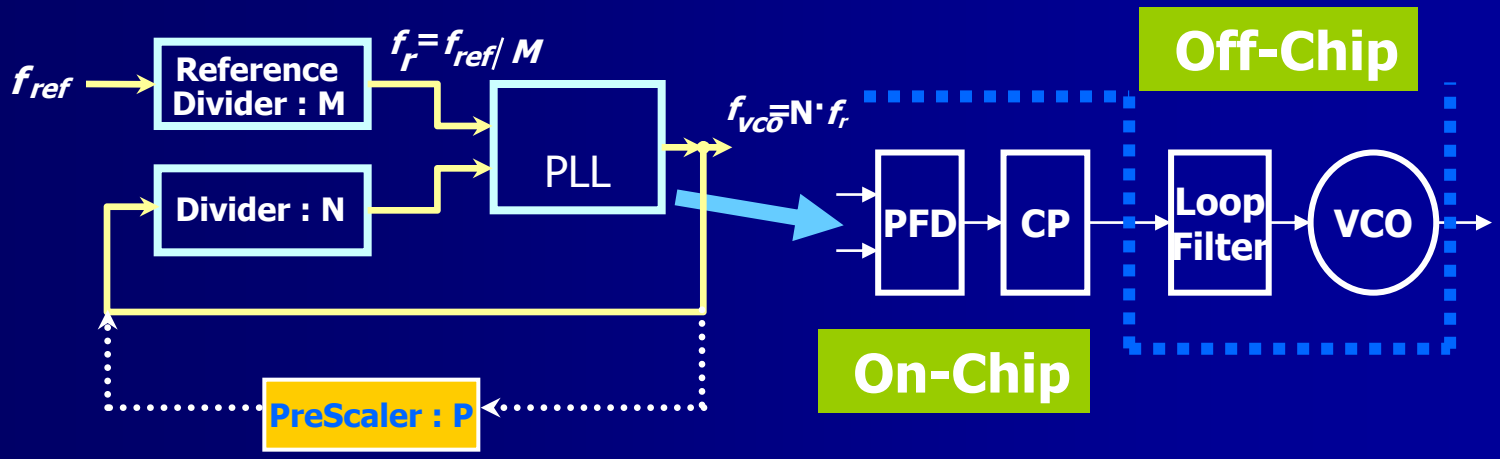
Frequency Synthesizer Implementation



Classification of Frequency Synthesizers

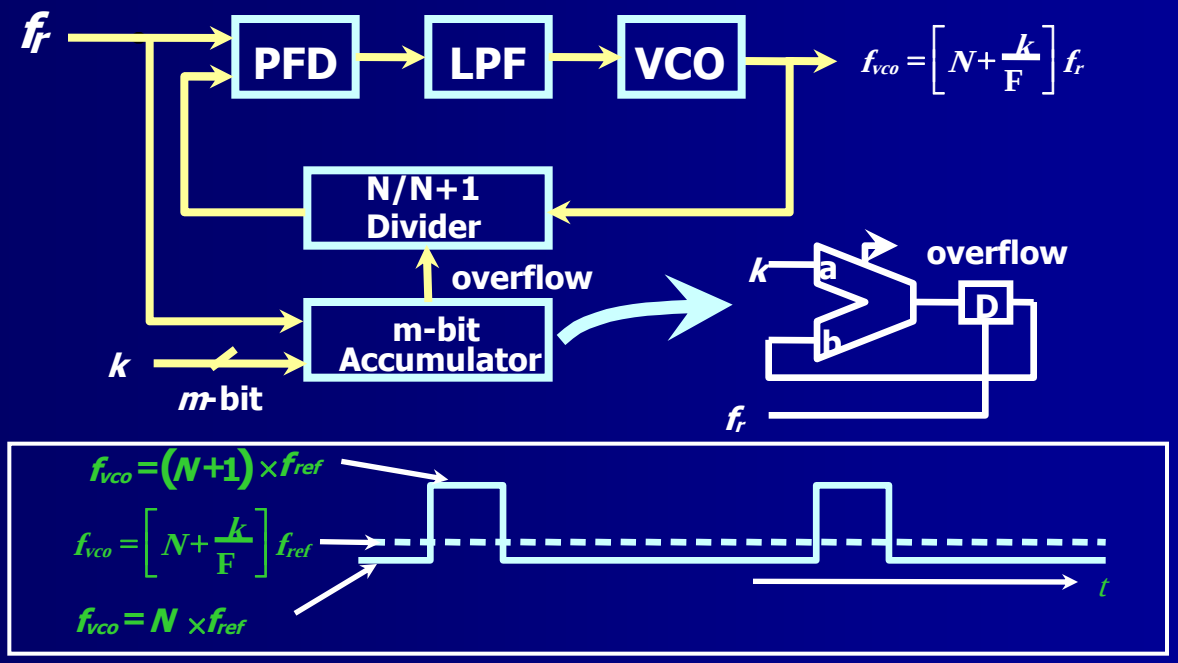


Integer-N PLL



- N is high for small channel spacing
- Slow switching time & poor phase noise characteristics ($\propto N^2$)

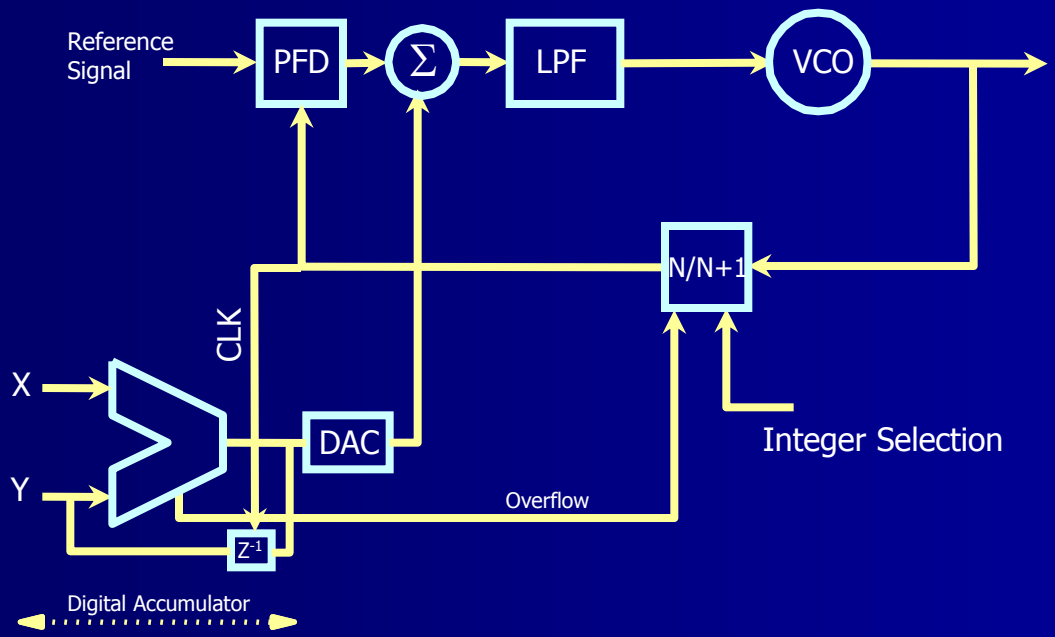
Fractional-N Frequency Synthesizer



- Problem : periodic change in instantaneous VCO frequency causes spurs at all multiples of $f = k/F \quad f_{ref}$

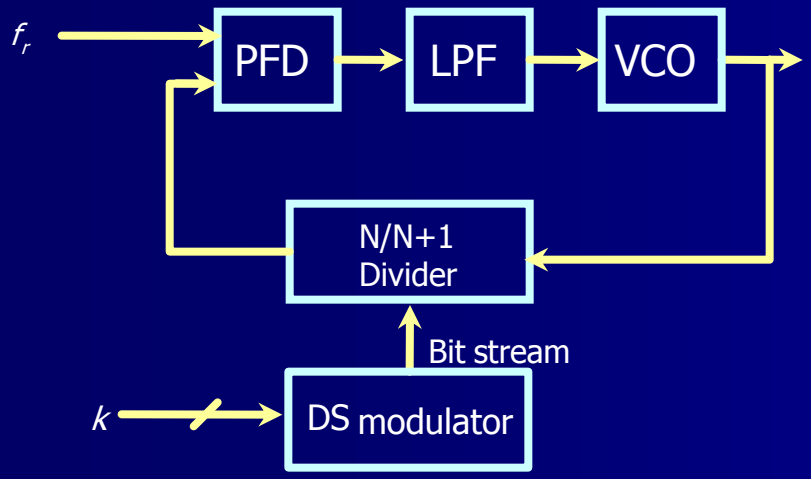
⟹ Fractional Spur Reduction Scheme required.

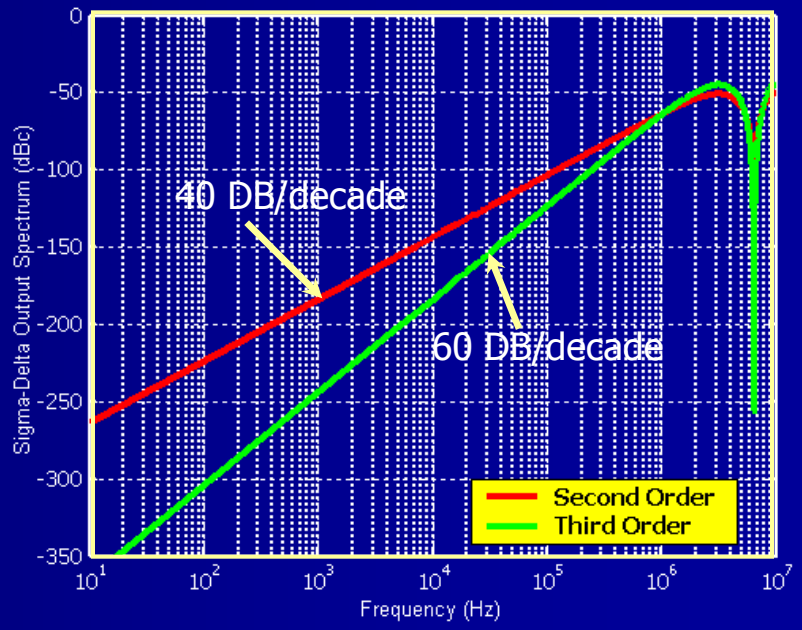
FN Synthesizer with Analog Compensation



- **Suppression is limited by analog mismatch**

Fractional-N Synthesizer using $\Delta\Sigma$ Modulation





- **Modulates divider ratio.**
- **Quantization noise problem.**

$$f_o = \underbrace{[N(z)+F(z)]f_{ref}}_{\text{Desired frequency}} + \underbrace{(1-z^{-1})^n Q_n(z) f_{ref}}_{\text{Frequency fluctuation}}$$

MASH 1-1-1 Architecture

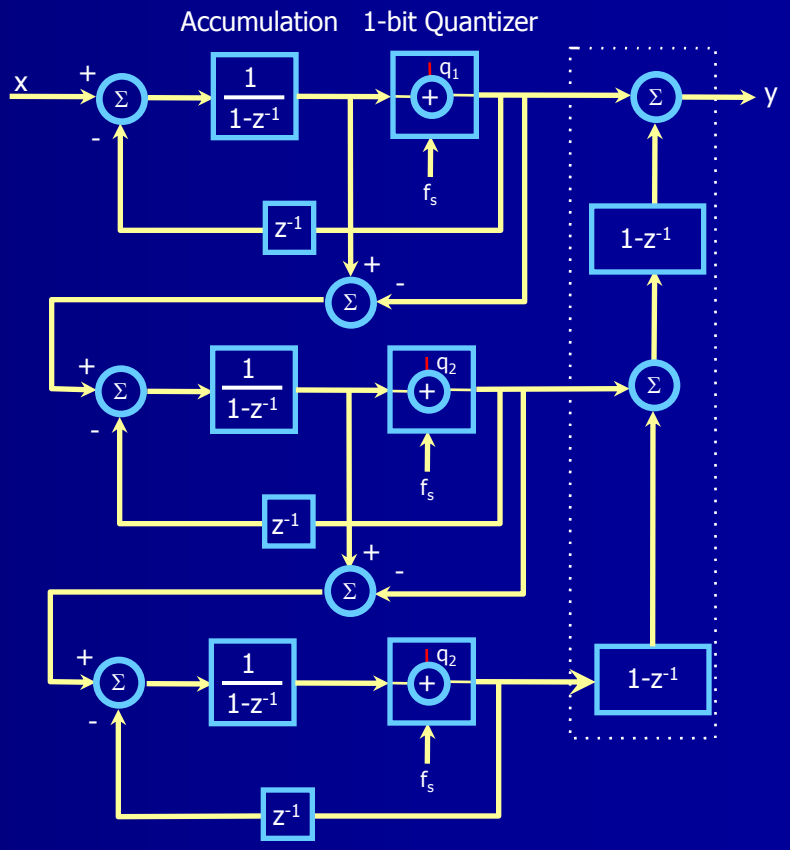
$$Y(z) = X(z) + (1 - z^{-1})^n . Q_n(z)$$

$$S(z) = \frac{(2\pi)^2}{12 . f_r} \left| 1 - z^{-1} \right|^{2(n-1)}$$

$$S(f) = \frac{(2\pi)^2}{12 . f_r} \left| 2 \sin\left(\frac{\pi . f}{f_r} \right) \right|^{2(n-1)}$$

For $f << f_r$

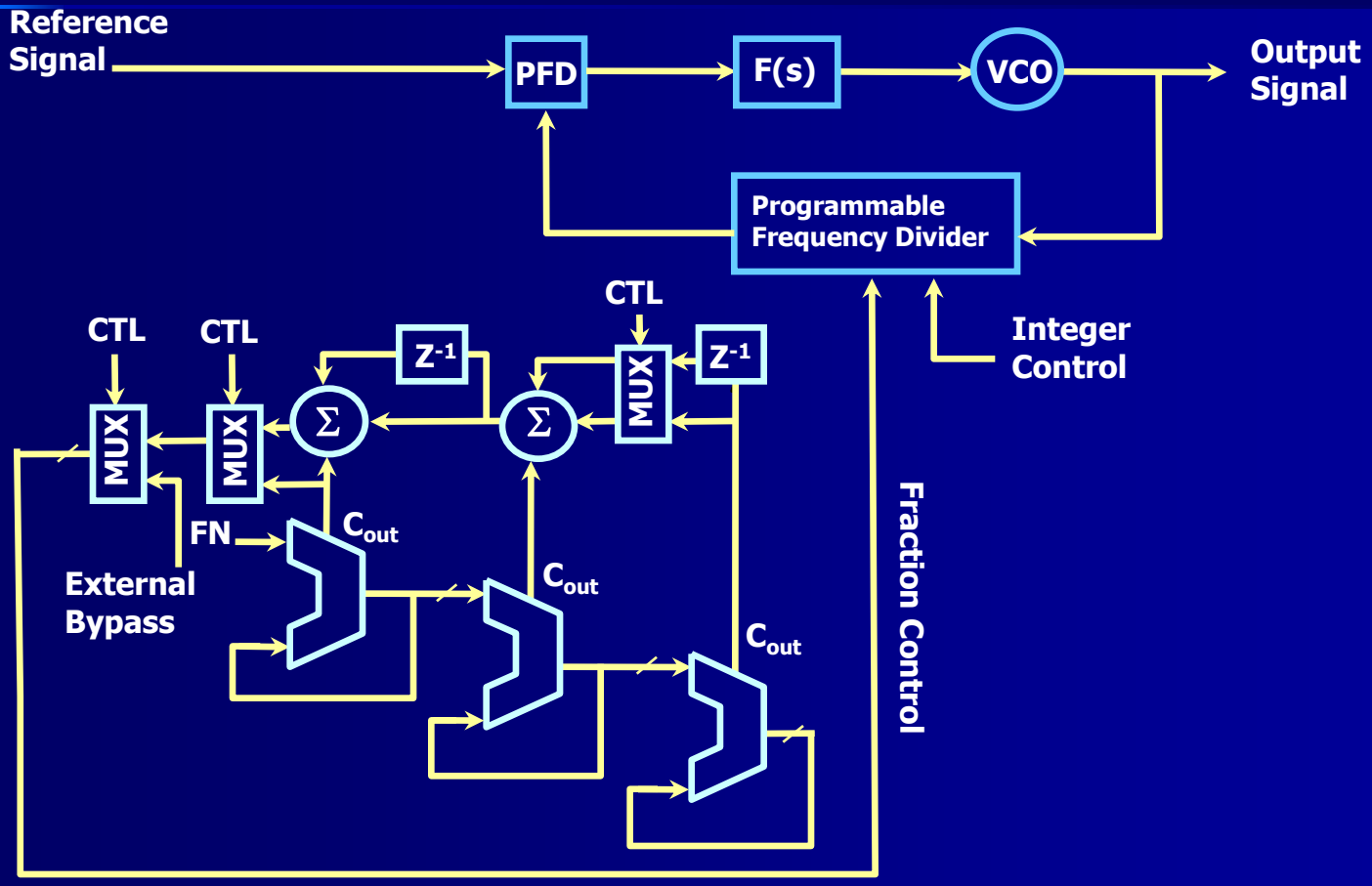
$$S(f) \approx \frac{(2\pi)^2}{12 . f_r} \left| 2 . \pi \left(\frac{f}{f_r} \right) \right|^{2(n-1)}$$



Outline

- Motivation
- Background
- Novel Fractional-N Frequency Synthesizers
- Novel Analog-to-Digital Architecture
- Conclusions

Fractional-N FS Using MASH 1-1-1



Programmable Frequency Divider

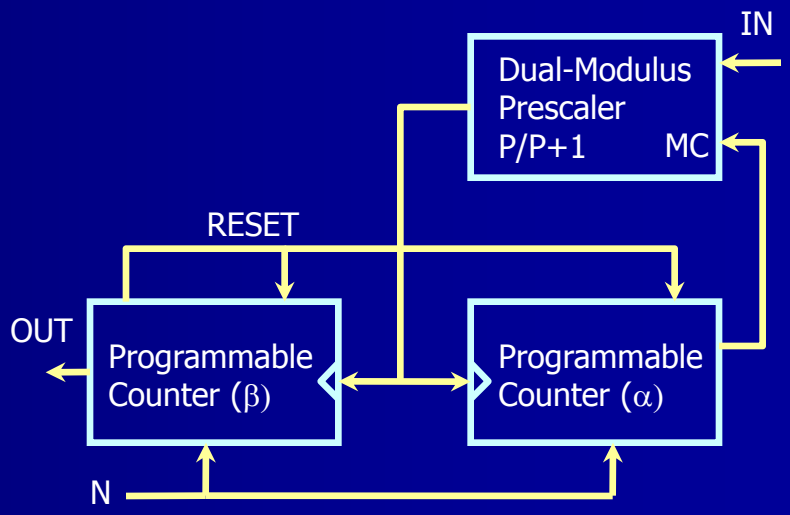
- The input is divided by (P+1) for α cycles and by P for (β-α) cycles thus giving the total division ratio of the divider as

  $\mathbf{N_{total} = \alpha(P+1) + (\beta-\alpha)P}$

  $\mathbf{= \beta P + \alpha}$

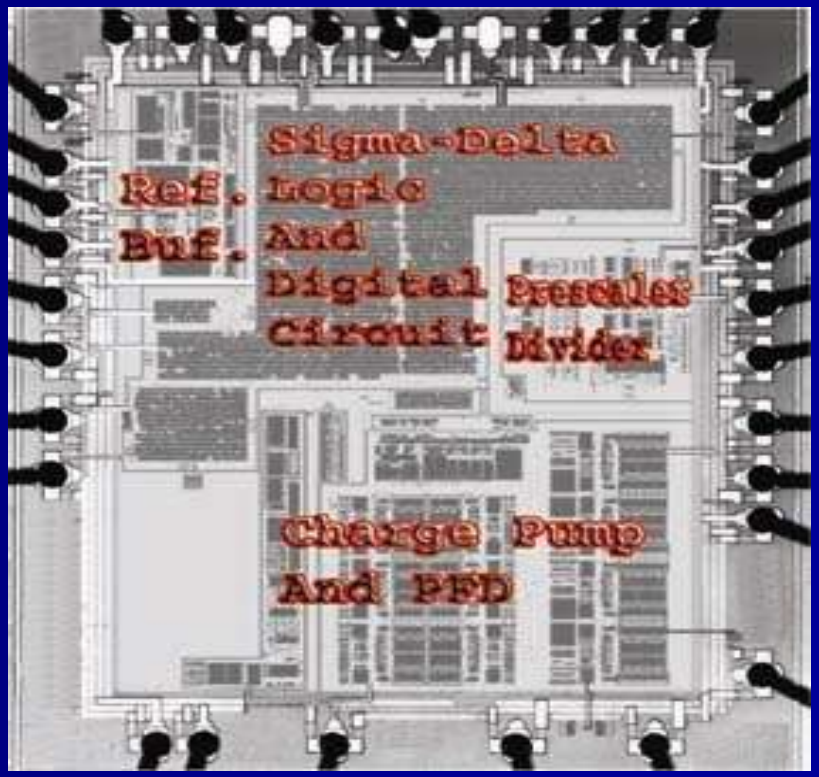
  where $\beta \geq \alpha$

- The smallest possible division ratio of a dual modulus prescaler is P(P-1)

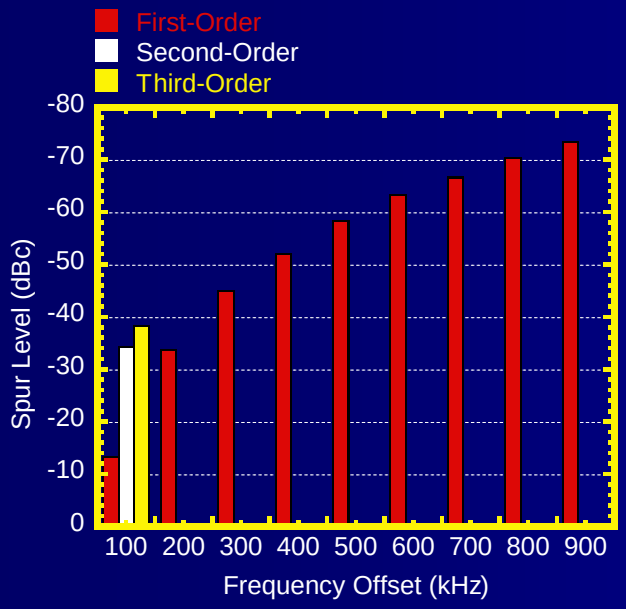


Fractional-N FS Using MASH 1-1-1

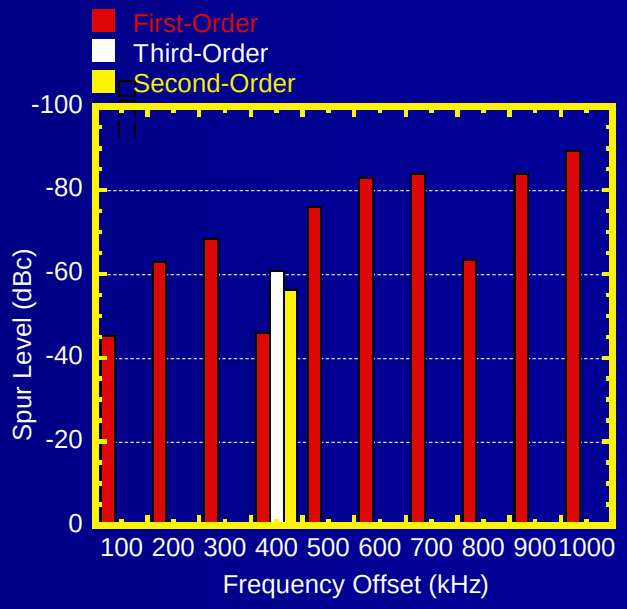
- Chip fabricated in 0.35μm BiCMOS
- Area=1.85x2.33mm^2



Measured Spurious Performance



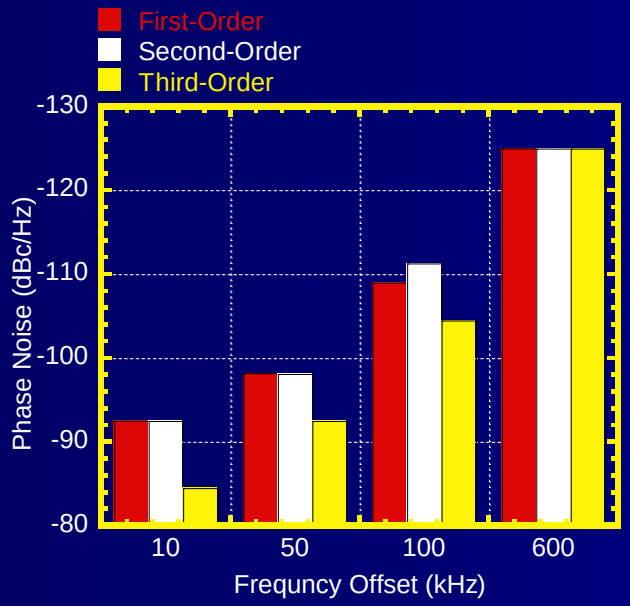
Spurs for 1/65 Fractional



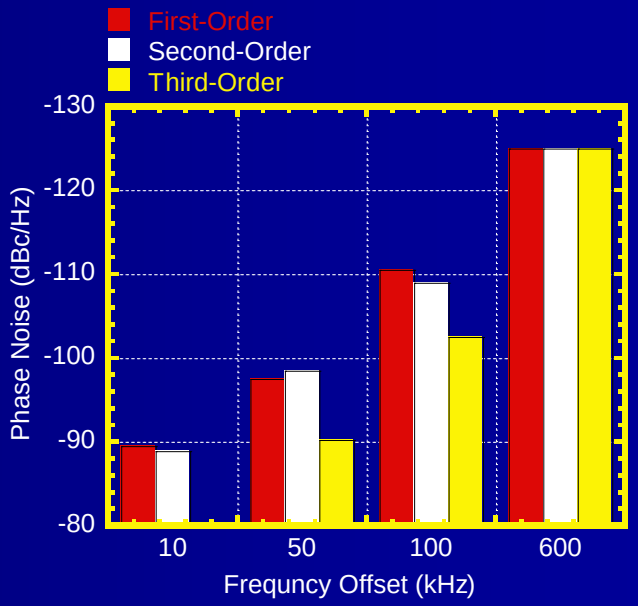
Spurs for 4/65 Fractional

- **f_{ref} = 6.5MHz**
- **Loop BW = 30kHz**
- **Fractionality = 65**

Measured Phase Noise Performance



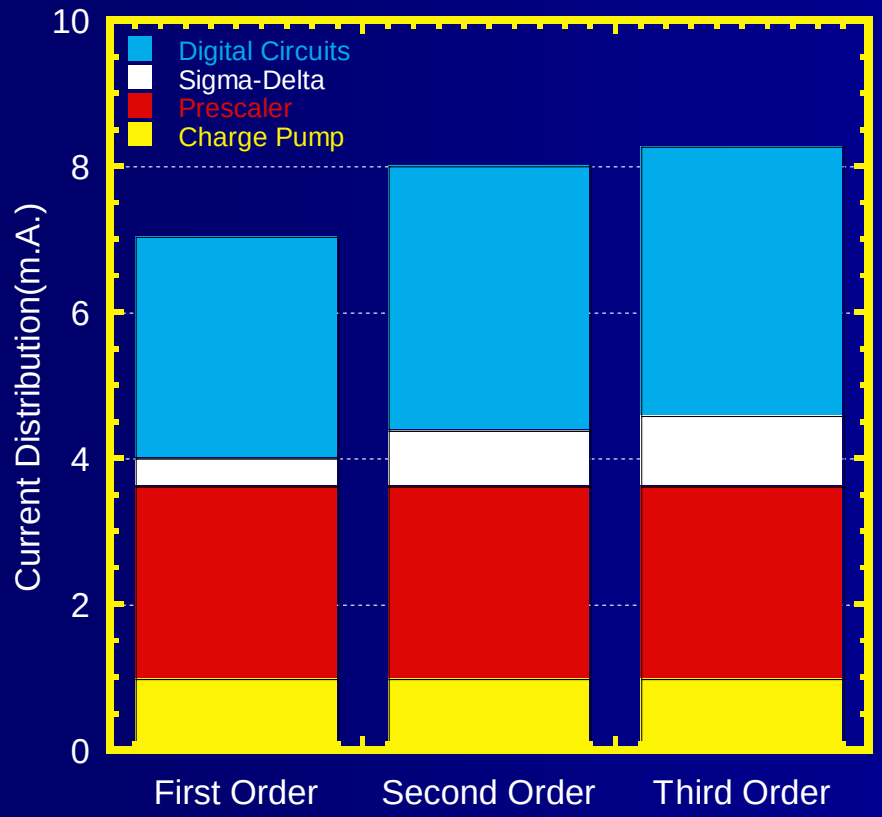
Phase Noise for 1/65 Fractional



Phase Noise for 4/65 Fractional

- **f_{ref} = 6.5MHz**
- **Loop BW = 30kHz**
- **Fractionality = 65**

Measured Current Distribution

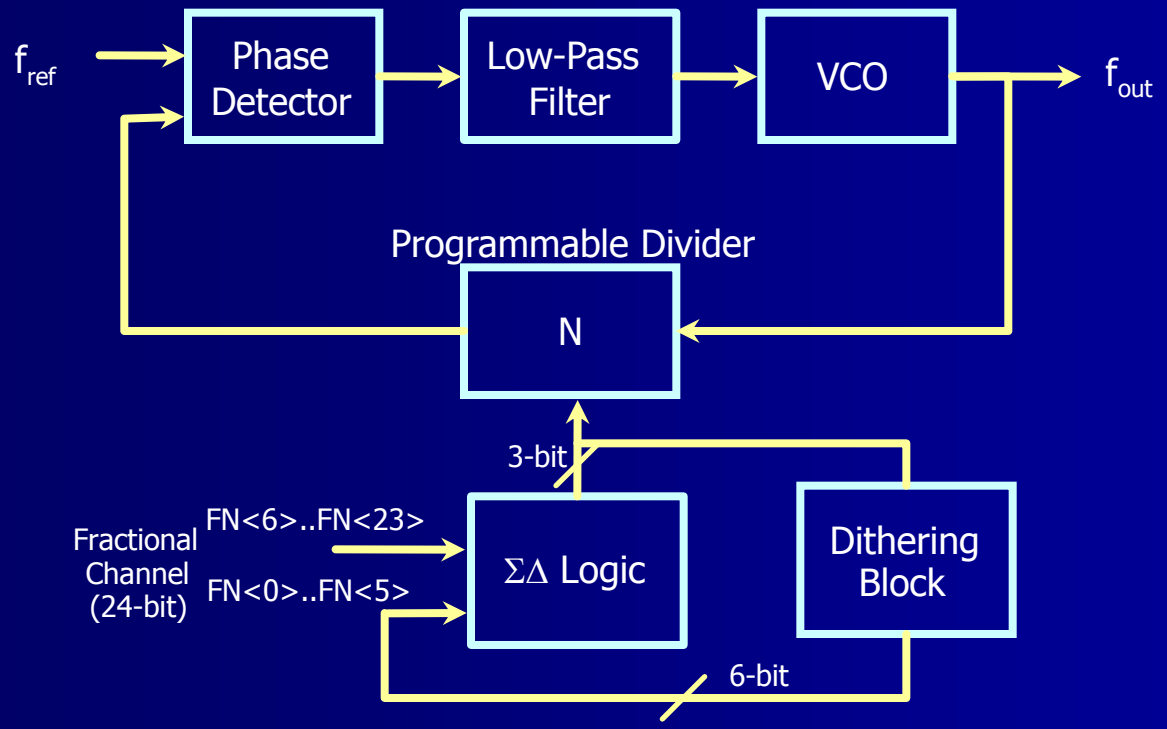


- f_{ref} = 6.5MHz
- Loop BW = 30kHz
- Supply Voltage = 3.3V

Experimental Results Summary

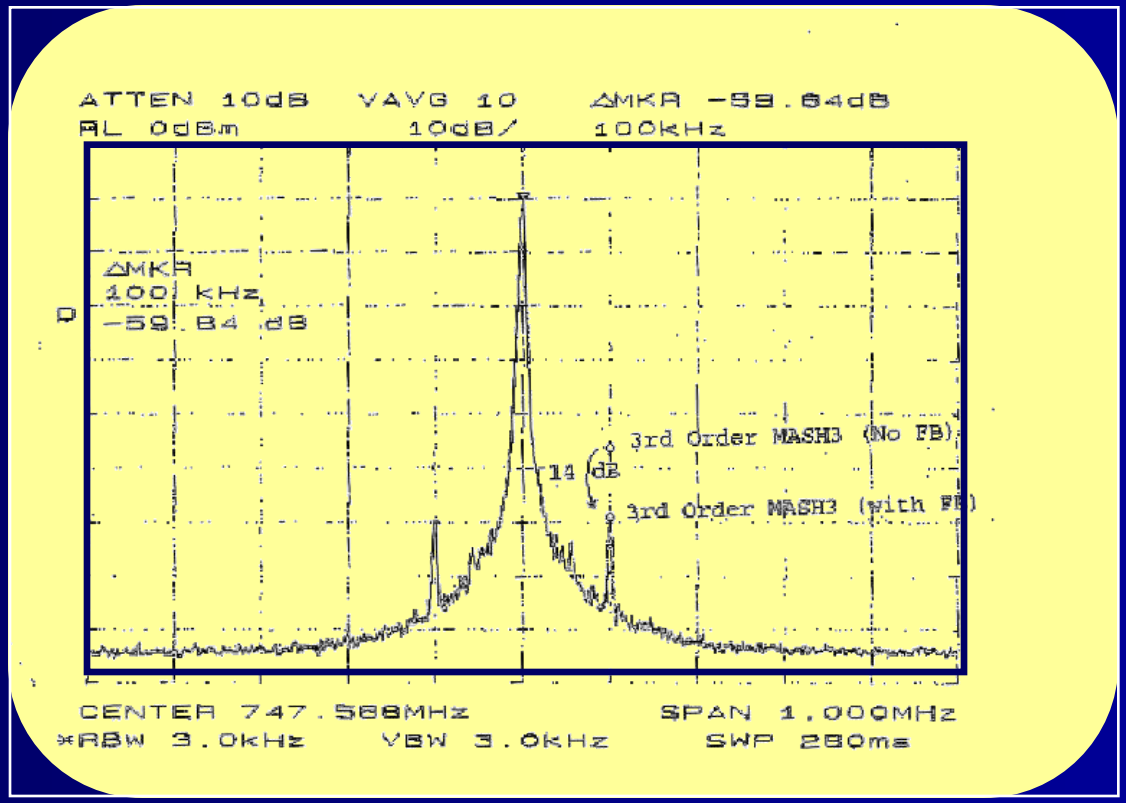
	GPRS	Measured
Phase Noise @ 10kHz (dBc/Hz)	-70	-80
Phase Noise @ 3MHz (dBc/Hz)	-123	-125
Power Supply (V)	-	2.5-5.0
Fractional Spurs @0.4MHz (dBc)	-54	-60
Power Consumption (mW)	-	27@3.3V
Lock Time (μs)	200	95
Frequency Range (MHz)	880-915	128-1200

Feedback ΔΣ FS



- **ΣΔ output is used as a dithering signal**

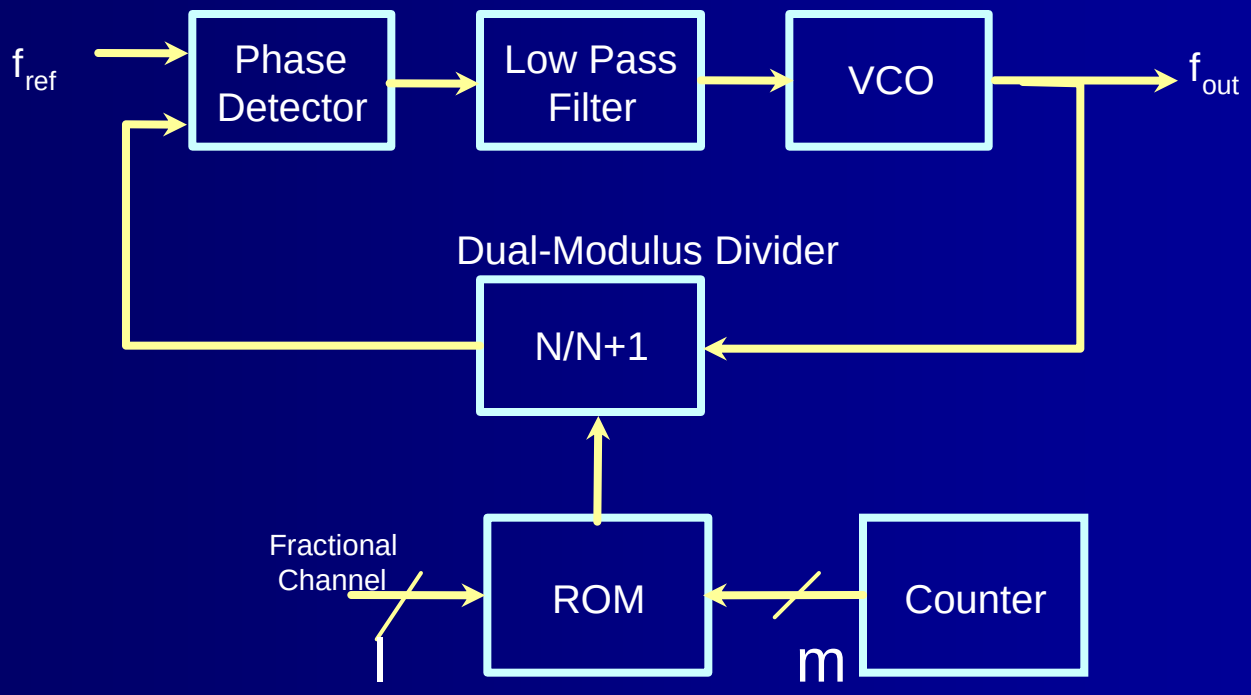
Measured Output Spectrum



- f_{ref} = 6.5MHz
- Loop BW = 30kHz
- Fractional Channel = 1/65

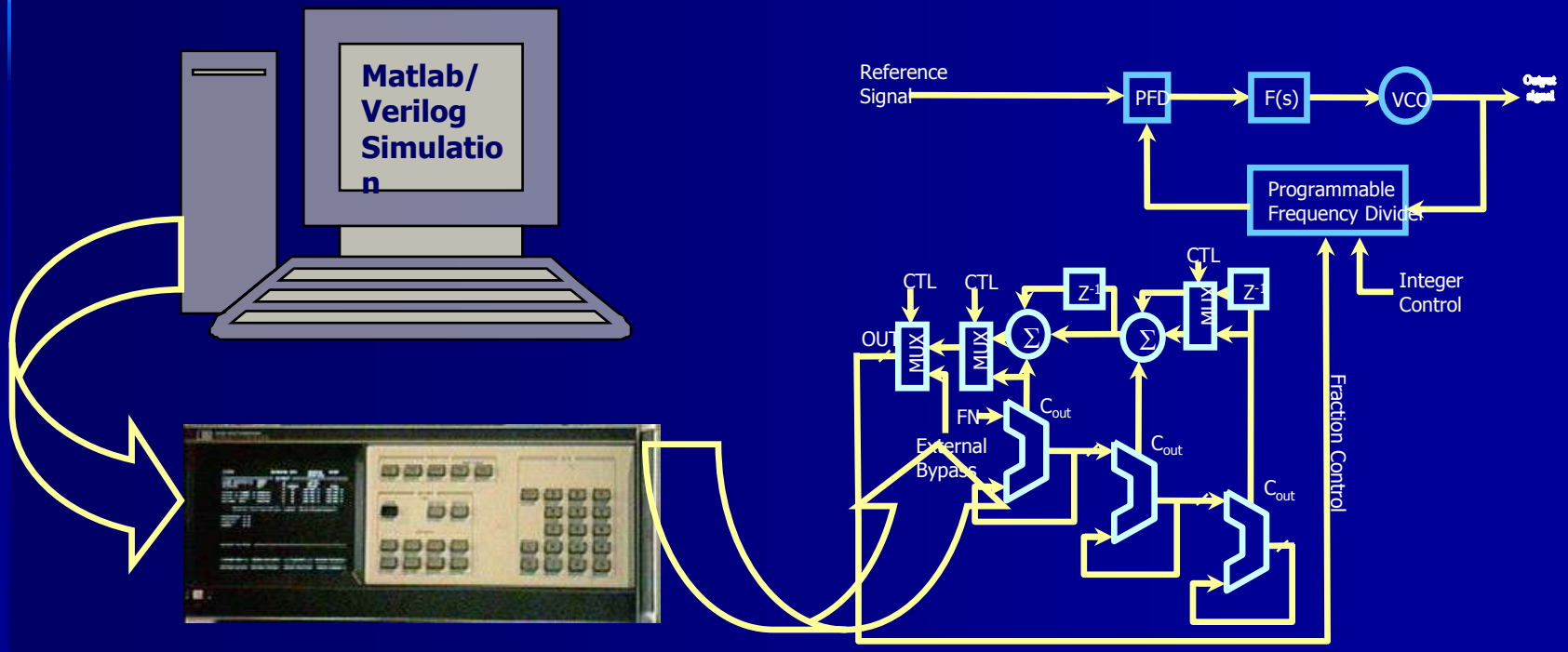
- 14dB Spur Reduction

ROM-Based FN Frequency Synthesizer



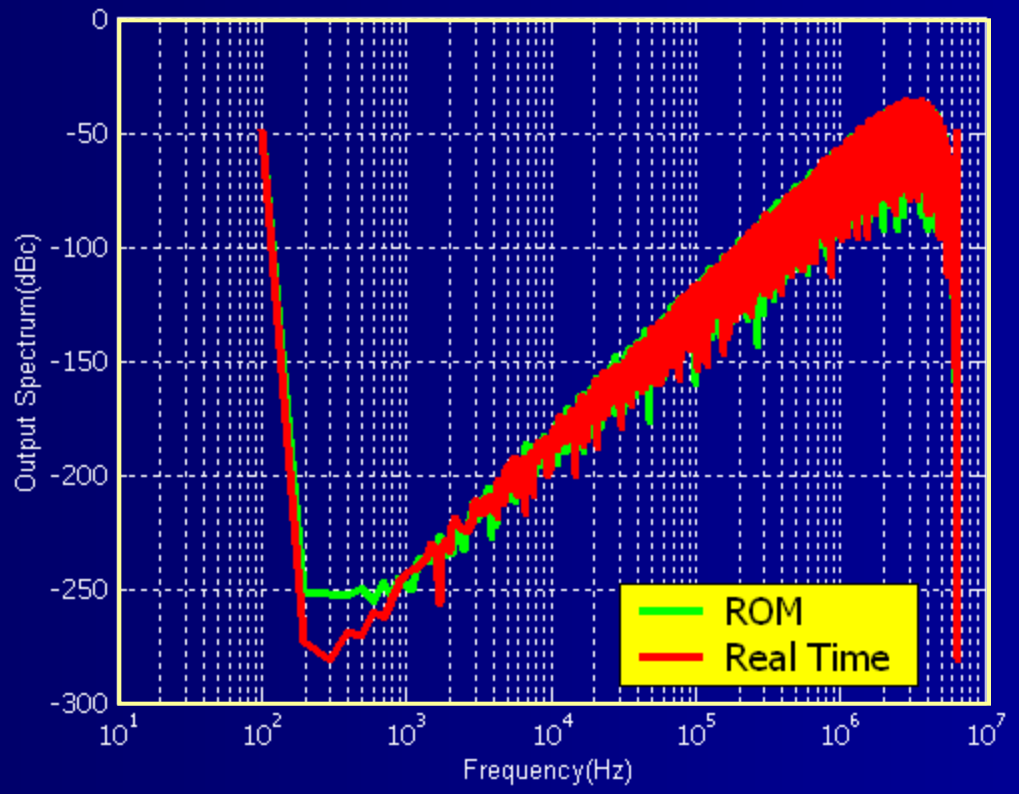
- **Guaranteed Stability**
- **Higher Operating ΣΔ Frequency**
- **Lower Power Dissipation**

Experimental Setup

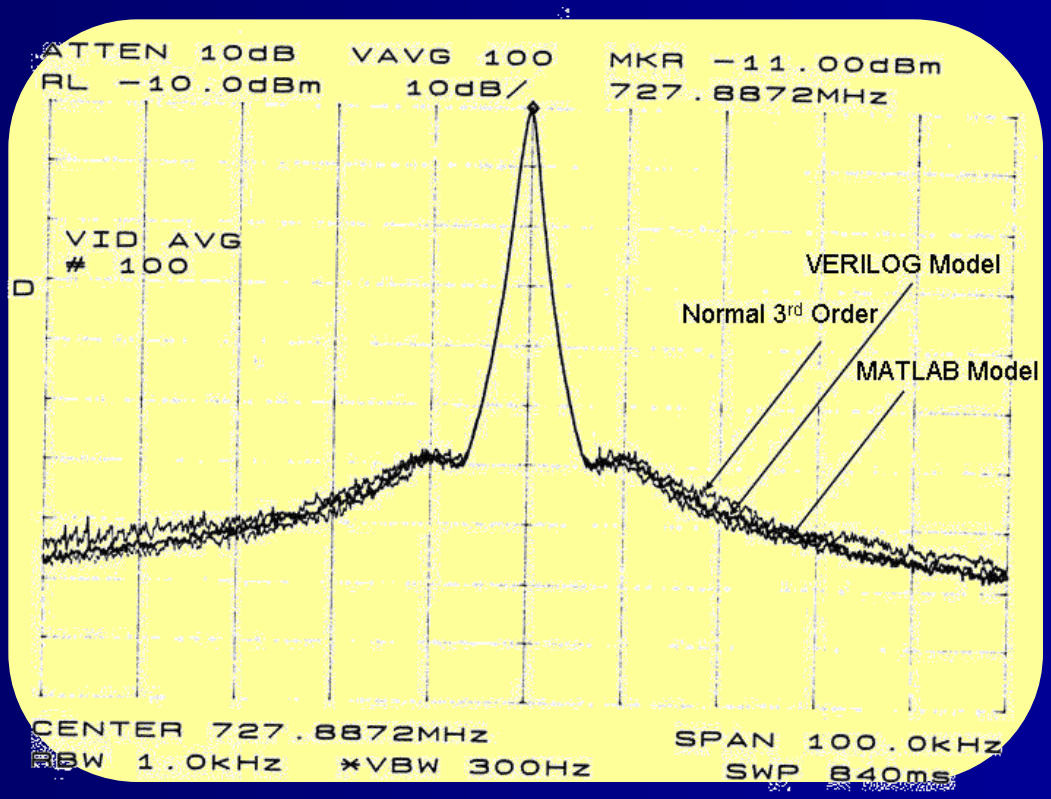


Data Generator (HP 8180A)

Simulated ΔΣ Output Spectrum

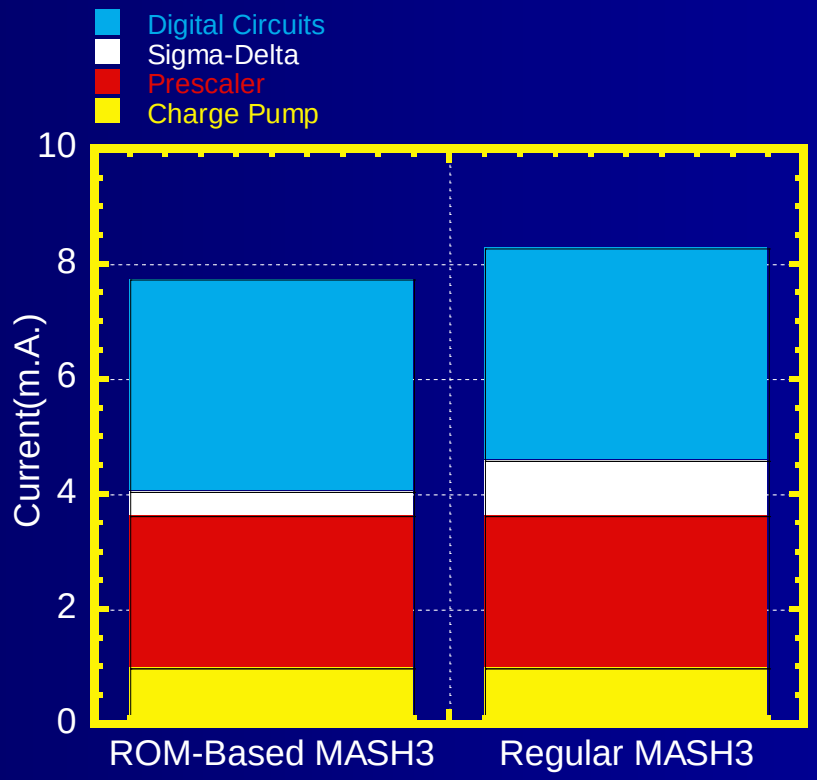


Measured Output Spectrum



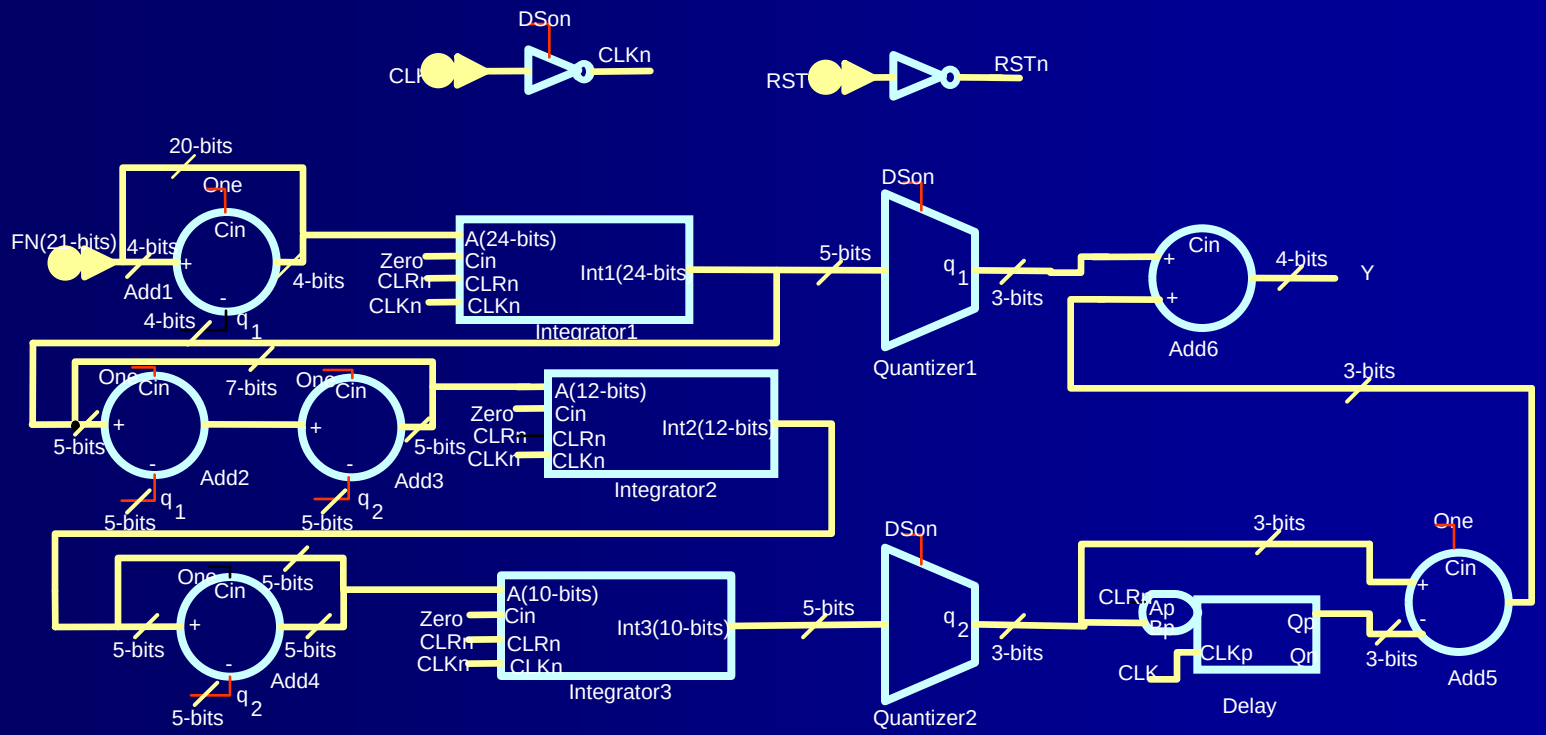
- f_{ref} = 6.5MHz
- Loop BW = 30kHz
- Fractionality = 65

Measured Current Distribution



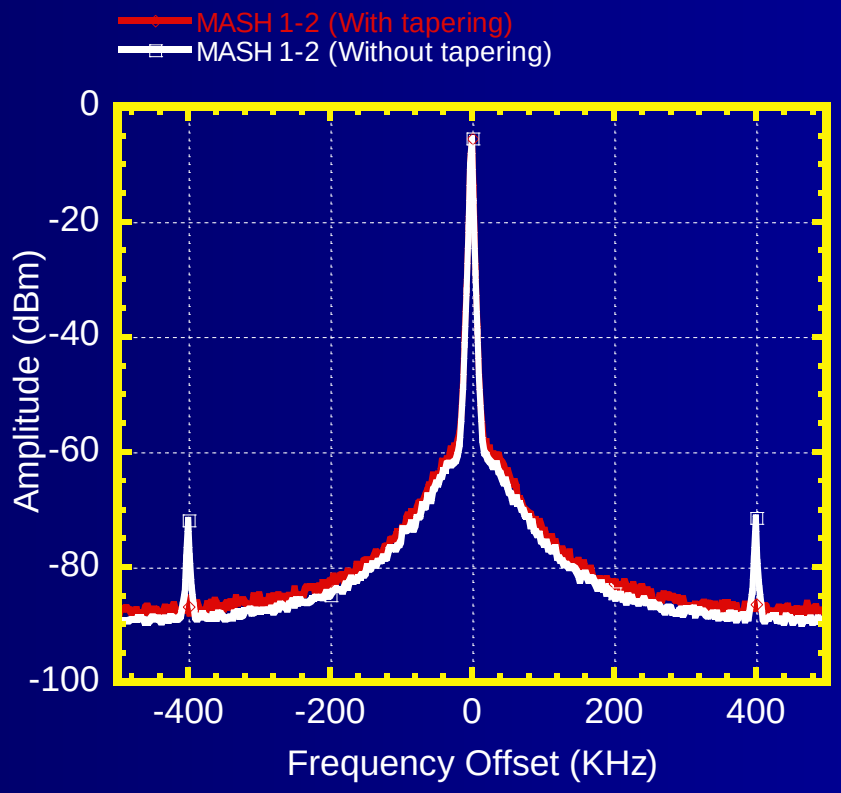
- **56% Power Reduction in ΔΣ**

Tapered MASH 1-2 ΔΣ FS



- Lower Power Dissipation
- Lower Spurs

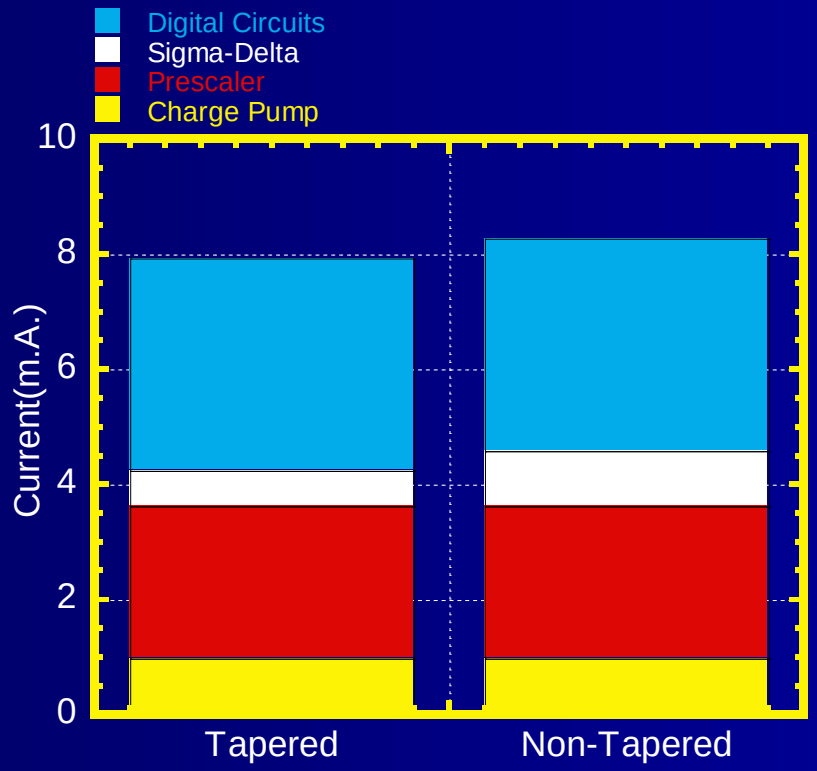
Measured Output Spectrum



- f_{ref} = 6.5MHz
- Loop BW = 30kHz
- Fractional Channel = 4/65

- 15dB Spur Reduction

Measured Current Distribution



- f_{ref} = 6.5MHz
- Loop BW = 30kHz
- Fractionality = 65

- 36% Power Reduction in ΔΣ

Outline

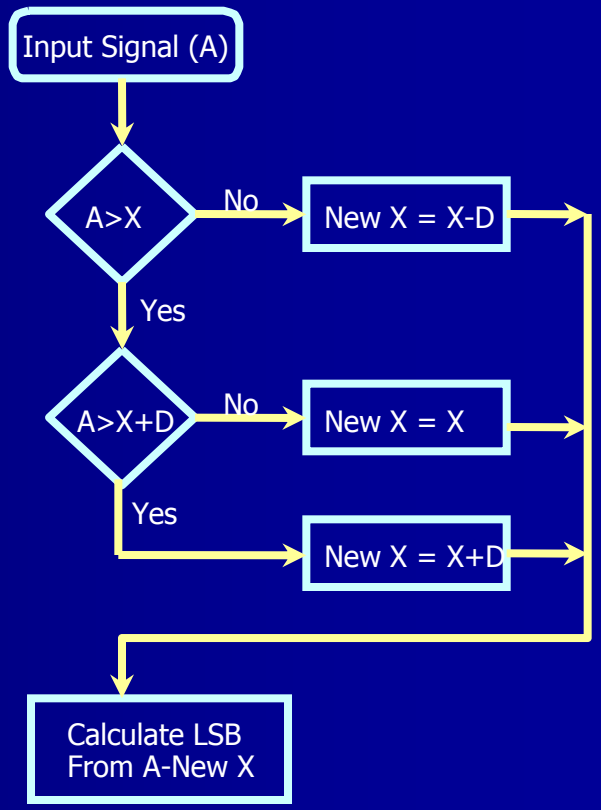
- Motivation
- Background
- Novel Fractional-N Frequency Synthesizers
- Novel Analog-to-Digital Architecture
- Conclusions

Analog-to-Digital Conversion

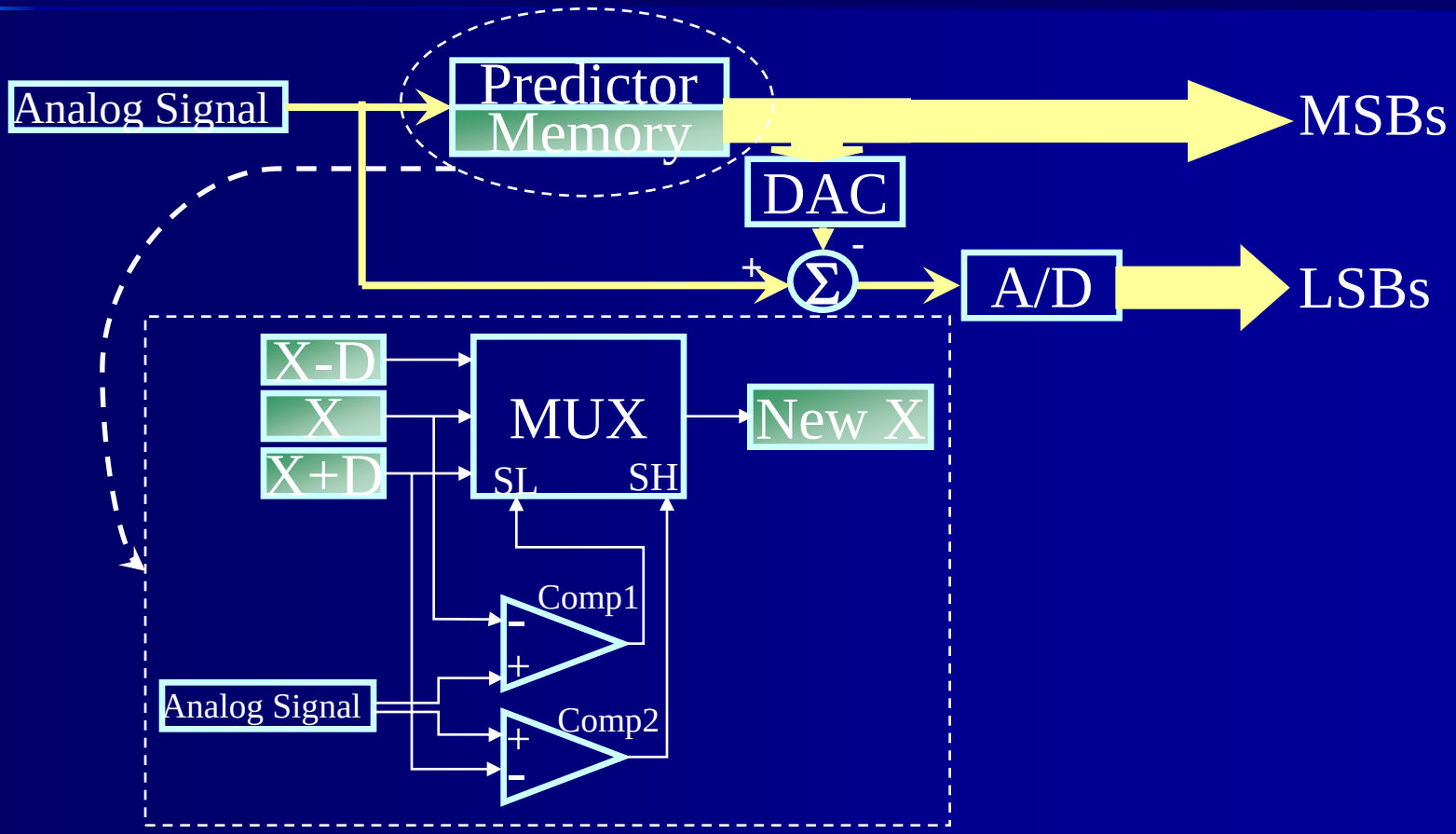
- Do we need all the resolution range in this case ?!

Algorithm Flow Chart

- A = New Sample
- X = Analog value corresponding to MSBs from the last sample
- D = 2^{-m} * Full scale voltage
- m = Resolution bits



Memory-Based A/D



Figures of Merit for A/D

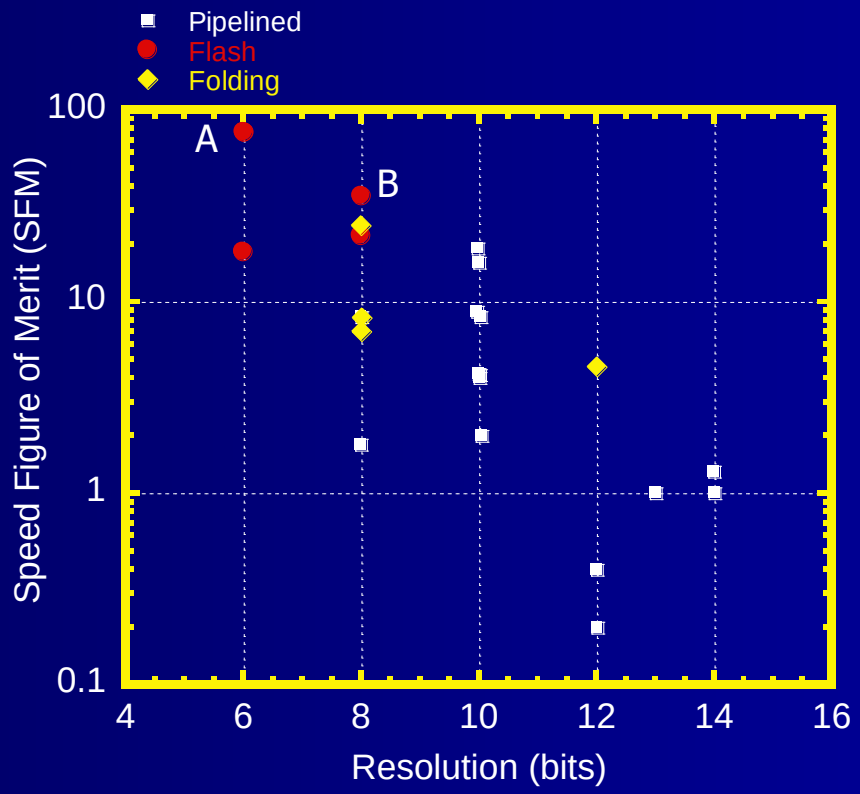
- Speed Figure of Merit
- Power Figure of Merit

$$SFM = \frac{SR}{f_c}.10^3$$

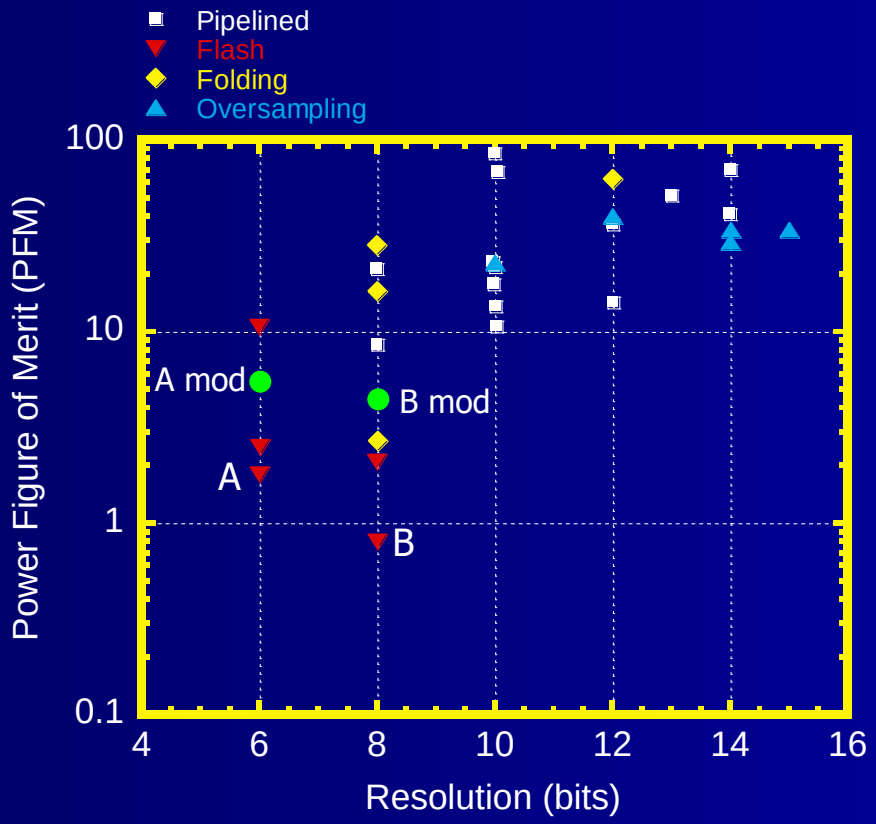
$$PFM = \frac{2^n \cdot SR}{f_c \cdot P}$$

  - SR = Sampling rate
  - f_c = Cutoff frequency
  - N = Resolution bits
  - P = Power dissipation

Speed Figure of Merit



Power Figure of Merit



Outline

- Motivation
- Background
- Novel Fractional-N Frequency Synthesizers
- Novel Analog-to-Digital Architecture
- Conclusions

Conclusions

- Enhancing the lock time, phase noise, and reference spurs are possible with fractional-N frequency synthesizers
- A 1.2 GHz fractional-N frequency synthesizer is presented with MASH architecture and pulse-swallowed dual-modulus divider, in 0.35μm BiCOMS
- Measured performance meets the GPRS requirements
  - Lock Time =95μs, in-band phase noise= -80 dBc/Hz, and out-of-band phase noise= -125 dBc/Hz at 3MHz
- $\Delta\Sigma$ output may be used as a dithering signal to reduce the spurs

Conclusions

- ROM-Based $\Delta\Sigma$ frequency synthesizers enhance the stability, speed, and power dissipation of the $\Delta\Sigma$ architecture
- Tapering the $\Delta\Sigma$ accumulators enhance the power dissipation, and reduce the spurs of the frequency synthesizer
- Using past history we can cut the required H/W for ADCs
- A memory-based ADC architecture is proposed, high level simulations verify the functionality and stability of the proposed architecture

Future Work

- Multi-Standard frequency synthesizers
- Power dissipation reduction in fractional-N frequency synthesizers
- Low phase noise VCO
- Integrating the VCO and the loop filter for monolithic solution
- Increasing the dynamic range of the memory-based ADC

Publications

- A. E. Hussein and M. I. Elmasry, "A ROM Based Fractional-N Frequency Synthesizer for Wireless Communication," in Proc. of Midwest Symposium on VLSI, August 2002, Tulsa, U.S.A.
- A. E. Hussein and M. I. Elmasry,"A Fractional-N Frequency Synthesizer for Wireless Communications," in Proc. of IEEE International Symposium on Circuits and Systems, vol.4, pp.513-516, May 2002, Arizona, U.S.A.
- A. E. Hussein and M. I. Elmasry, "Low Power Analog-to-Digital Converter for Wireless Communication," in Proc. of 10th ACM Great Lakes Symposium on VLSI, March 2000, Chicago, U.S.A.
- A. E. Hussein, M. A. Hasan, and M. I. Elmasry, "A New Algorithm for the Division in the Residue Number System (RNS) For Low Power Applications," in Proc. of CCECE'98, vol.1, pp.205-208, May 1998, Waterloo, ON, Canada.
- A. E. Hussein and M. I. Elmasry,"A Novel Fractional-N Frequency Synthesizers for Wireless Communications," IEEE Journal of Solid-State Circuits (in preparation)
- A. E. Hussein and M. I. Elmasry, "A Low Power Analog-to-Digital Converter for Wireless Communication," IEEE Transactions on Circuits and Systems II (in preparation)