Low Power High Speed Analog-to-Digital Converter for Wireless Communications

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Abstract

A new ADC architecture is devised. This architecture is memory based, in which the last sample is used to predict the current one, resulting in both power dissipation and energy reduction. The low power dissipation is a vital factor when we consider the chip reliability and integrity. The low energy consumption is a critical factor when we deal with battery operated devices like PCSs. This technique may also be used to extend the attainable flash converter resolution by pre-calculating the most significant bits.