EE 200 DIGITAL LOGIC DESIGN EXPERIMENT #7

ADDERS, SUBTRACTORS AND MAGNITUDE COMPARATORS

Objectives:

- To construct and test various adders and subtractor circuits.
- To construct and test a magnitude comparator circuit.

Apparatus:

- IC type 7486 quad 2-input XOR gates
- IC type 7408 quad 2-input AND gates
- IC type 7404 HEX inverter
- IC type 7483 4-bit binary adder
- IC type 7485 4-bit magnitude comparator.

Theory:

See Sections 1-5,4-3,5-2,5-4 of your textbook.

a) *Addition:*

IC type 7483 is a 4-bit binary adder with fast carry. The pin assignment is shown in Fig 1. The two 4-bit input binary numbers are A_1 through A_4 and B_1 through B_4. The 4-bit sum is obtained from S_1 through S_4. C_i is the input carry and C_o the out carry. This IC can be used as an adder-subtractor as a magnitude comparator.

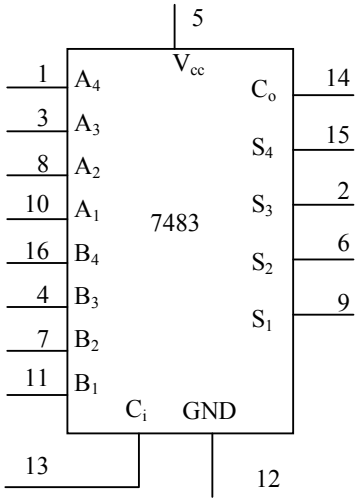
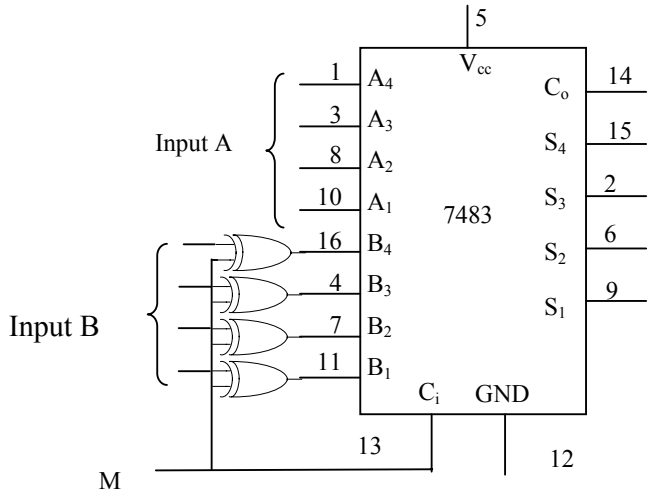


Fig.1 IC type 7483 4-bit adder

b) *Subtraction:*

The subtraction of two binary numbers can be done by taking the 2's complement of the subtrahend and adding it to the minued. The 2's complement can be obtained by taking the 1's complement and adding 1.

To perform A - B, we complement the four bits of B, add them to the four bits of A, and add 1 to the input carry. This is done as shown in Fig 2.



M = 0 for add and M = 1 for subtract

Fig. 2 4-bit adder/subtractor

Four XOR gates complement the bits of B when the mode select M = 1 (because $x \oplus 1 = x'$) and leave the bits of B unchanged when M = 0 (because $x \oplus 0 = x$) thus, when the mode select M is equal to 1, the input carry C_i is equal to 1 and the sum output is A plus the 2's complement of B. When M is equal to 0, the input carry is equal to 0 and the sum generates A + B.

c) *Magnitude comparison*

The comparison of two numbers is an operation that determines whether one number is greater than, equal to, or less than the other number.

The IC 7485 is a 4 bit magnitude comparator. It compares two 4-Bit binary numbers (labeled as A&B) generates an output of 1 at one of three outputs labeled A > B, A < B, A = B. Three inputs are available for cascading comparators. see Fig.3.

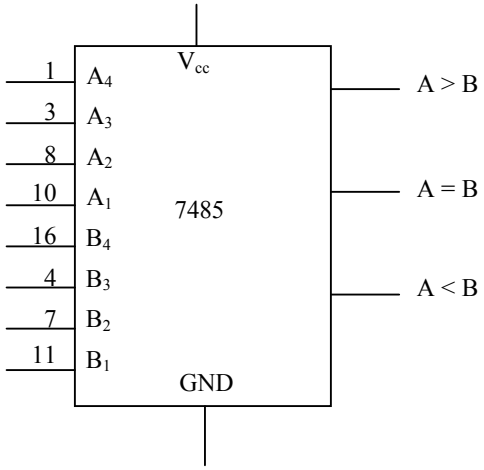


Fig. 3 4-bit magnitude comparator

Procedure:

a) Design using LogicWorks a half adder circuit using only XOR gates and NAND gates. Then during the Lab construct the circuit and verify its operation.
b) Design using LogicWorks a full adder circuit using only XOR gates and NAND gates. Then during the Lab construct the circuit and verify its operation.
c) Use IC 7483 to add the two 4-bit numbers A and B shown in Table1. In LogicWorks, select the chip 74-83 and use Binary switches for the bits of the two numbers and the input carry and use Binary Probe for the sum and carry out.

Table 1.

A3	A2	A1	A0	B3	B2	B1	B0	Sum				Carry out
1	0	0	1	0	0	1	0					
0	1	1	0	1	0	1	1					
1	1	0	0	1	0	1	0					

Input carry Ci is taken as logic 0. Show that if the input carry is 1, it adds 1 to the output sum.

In the Lab use switches S1-1 to S1-8 for the two numbers and use the SPDT S2 for the input carry Ci. For sum and carry out, use LED-1 to LED-5.

d) Connect the adder-subtractor circuit as shown in Fig 2. Perform the following operations and record the values of the output sum and the output carry C_o.

Table 2.

Decimal A B	**Output sum**				**Carry Out C_o**
9 + 5					
9 - 5					
9 + 13					
9 - 9					
10 + 6					
6 - 10					

- Show that C_o =1 when sum exceeds 15.
- Comment on sum and C_o for the subtraction operations when A > B and A < B.

e) Use IC7485 to compare the following two 4 bit numbers A and B. Record the outputs in table 3. Note that in LogicWorks you need to connect (A = B) input to logic 1 (as an indication that previous stages are equal in multi-digit numbers) for correct results while this is not necessary for the hardware.

Table 3.

A	**B**	**Outputs**
1001	0110	
1100	1110	
0011	0101	
0101	0101	

f) A magnitude comparator can be constructed by using a subtractor as in Fig 2. and an additional combinational circuit. This is done with a combinational circuit which has 5 inputs S_1, S_2, S_3, S_4, and C_o, and three outputs X, Y, Z see Fig.4

X = 1 if A = B Where S = 0000

Y = 1 if A < B Where C_o = 0

Z = 1 if A > B Where C_o = 1 S ≠ 0000

Design and construct this logic circuit with minimum number of gates. Check the comparator action using Part (e). In the Lab verify your LogicWorks simulation.

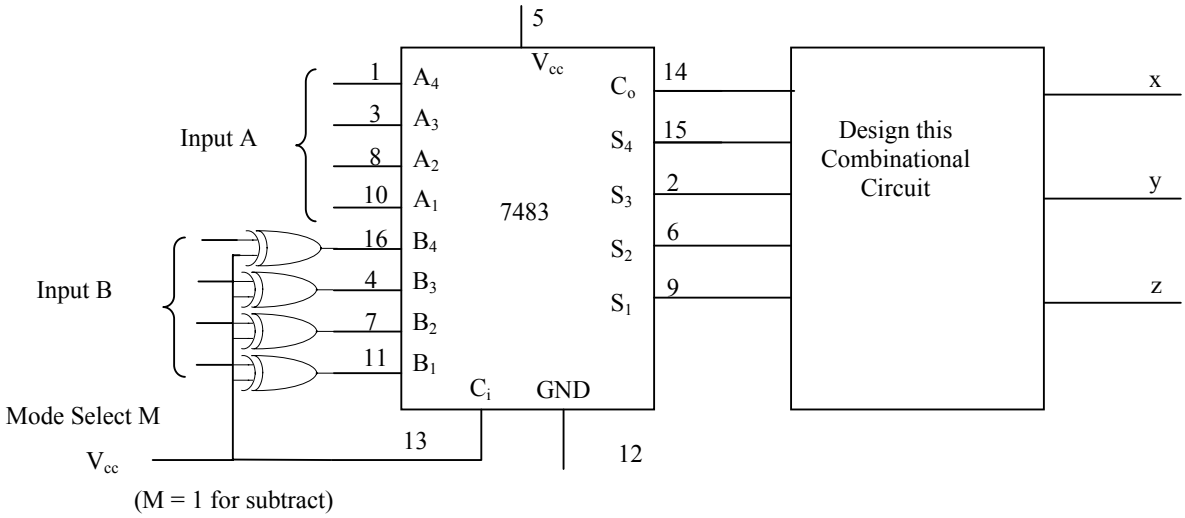


Fig.4 A magnitude comparator using a subtractor