EXPERIMENT 1

1. Introduction to Digital Design

1.1 Objectives

1. Binary Logic Basics.

2. Logic Gates Basics (Signal voltages for 0 &1, Logic Operations: AND, OR, NAND, NOR and NOT and their Truth Tables)

3. Familiarize with IC's (IC Pins: inputs, outputs, VCC & GND, applying inputs and monitoring outputs)

4. Partial familiarization with FPGA board, pins, switches, LEDs and power supply connections.

5. Verify Basic gates operation

1.2 Overview

The purpose of this lab is to get familiar with binary logic, logic gates and their truth tables. It also exposes you to integrated circuits (ICs).

To achieve this, you will be interfacing ICs with the bread-board available on the FPGA board. You will also be using on-board switches, LEDs and power supply pins to verify the truth tables of some logic gates.

1.3 Design Description

In COE 200 lab, you are required to work on digital circuits. Digital circuits are hardware components that are implemented using transistors and interconnections in complex semiconductor devices called *integrated circuits*. Digital circuits work in binary logic domain which uses two discrete values, **TRUE** (High) and **FALSE (Low)**. We can also refer to these values as **1(High)** and **0 (Low)**.

Logic Gates are basic building blocks of digital circuits. Using these building blocks, complex functions or larger digital circuits can be built. Examples of the basic logic gates are **AND, OR, NOT, NAND and NOR**. A complex gate such as an **XOR** gate can be built out of these basic gates. An example of the larger complex digital circuit is the digital clock.

The operation of a logic gate can be described using a *truth-table*. A truth-table is a tabular listing of all possible inputs and corresponding outputs of a logic gate. Table 1.1, Table 1.2, and Table 1.3 show truth tables of the AND, OR and NOT (Inverter) gates

Table 1.1: Truth table of an AND gate.
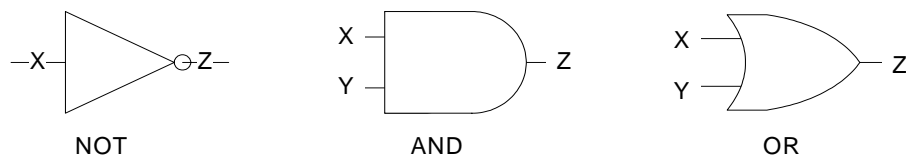
Input 1 (X)	Input 2 (Y)	Output (Z)
0	0	0
0	1	0
1	0	0
1	1	1

Table 1.2: Truth table of an OR gate.

Input 1 (X)	Input 2 (Y)	Output (Z)
0	0	0
0	1	1
1	0	1
1	1	1

Table 1.3: Truth table of a NOT (Inverter) gate.

Input (X)	Output (Z)
0	1
1	0

The graphical symbols used to designate the three types of gates (AND, OR, and NOT) are shown in Figure 1.1.

Figure 1.1: Basic logic gates graphics symbols..

These gates are encapsulated in black boxes and are called integrated circuits (ICs). Each IC or chip has an ID number that can be referenced in IC Data Book. From the book, you can get the pin configuration of that chip.

A sample IC layout of a 4081 chip is shown in Figure 1.2. The IC contains four 2-input AND gates. The input and output of the gates are wired to a particular pin as shown in the figure. The pin locations for power (i.e. Vdd - pin 14) and Ground (i.e GND -pin 7) are also shown. Also note a notch in the middle top side of the IC shown as a square in the figure. The numbering starts from the left of that notch.
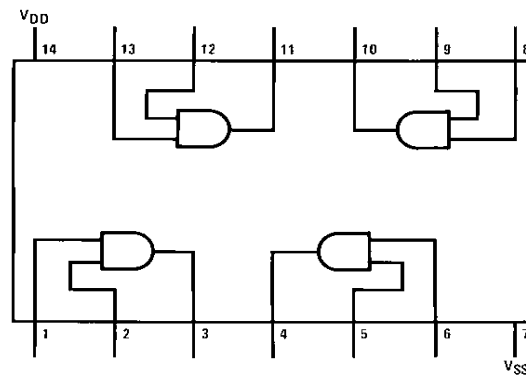
Figure 1.2: Quadruple 2-input AND gate.

ICs must be provided with power and ground connections. In complex ICs more than one pin can be dedicated for power (Vdd) as well as ground. In the simpler gates that we will be using in this experiment, the ICs require only one pin for power (Vdd) and another for ground (GND). The power supply (Vdd) voltage is typically +5 Volts, 3.3 Volts or 2.5 Volts. The ground which is the reference node is typically connected to 0 Volts. For more information on other ICs, you may refer to the data book.

1.4 Pre-lab

1. Read the experiment
2. Derive the truth table of the NAND and NOR gates (NAND is an AND followed by an inverted)
3. Refer to Chapter 2 in your text book.
4. Make a logic diagram for 4-input AND gate using 2-input AND gates of 4081 IC.

1.5 In-lab

1. You are required to build a 4-input AND gate.
2. Use one CMOS AND (4081) chip as in Figure 1.2.
3. Use the IC tester to test the 4081 chip.
4. Place the chip on the bread board of the FPGA board.
5. Connect a wire from the VDD pin on the J1 connector to the bread board.
6. Connect pin 14 (Vcc) of the chip to the VDD on the board.
7. Connect a wire from the GND pin on the J1 connector to the bread board.
8. Connect pin 7 (GND) of the chip to the GND on the board.
9. Build your logic diagram by making appropriate connections.
10. Use SW1, SW2, SW3, SW4 input pins on the J1 connector as your inputs to build a 4 input AND gate.
11. Connect the gate output to LD1 on the J1 connector of the digilab board.
12. Use the switches on the board to verify your gate.

1.6 Post-lab

1. Submit the truth table of the 4 input AND gate
2. Draw a circuit diagram of your implementation of the 4 input AND gate

1.7 Bonus-Stuff

1. Draw the graphic symbol and logic diagram for NAND and NOR gates using AND, OR and NOT gates
2. How can you build a 4 input NAND gate using the above circuit? Use additional gate(s) if required.