# GATS: A Novel Hybrid Algorithm for Cell Placement in VLSI Circuit Design

Sadiq M. Sait     Mahmood R. Minhas

Department of Computer Engineering
King Fahd University of Petroleum & Minerals
Dhahran 31261, Saudi Arabia
E-mail: {sadiq, minhas} @ ccse.kfupm.edu.sa

December 28, 2002

## 1   Abstract

This paper addresses the optimization of cell placement step in VLSI circuit design [1]. A novel hybrid algorithm is proposed for performance and low power driven VLSI standard cell placement. The above problem is of multiobjective nature since three possibly conflicting objectives are considered to be optimized subject to the constraint of layout width. These objectives are power dissipation, timing performance, and interconnect wire length. It is well known that optimizing cell placement for even a single objective namely total wire length is a hard problem to solve. Due to imprecise nature of objective values, fuzzy logic is incorporated in the design of aggregating function. The above technique is applied to the placement of ISCAS-89 benchmark circuits and the results are compared with those obtained from individual application of GA and TS on this problem.

## 2   GATS: A Hybrid of Genetic Algorithm and Tabu Search

Hybrid algorithms combine features from various heuristics as an effort to develop efficient techniques for solving hard optimization problems [2]. In the scope of the present work, hybridization refers to mixing of good characteristics from several iterative algorithms. The choice of iterative algorithms to be hybridized needs some careful analysis of the underlying problem and the characteristics of individual candidate algorithms. The application of an individual algorithm to the problem may give an insight of its suitability to the problem. If the results of application of the individual algorithms are

encouraging, then their hybridization is expected to produce even better performance in many cases.

Genetic Algorithm (GA) and Tabu search (TS) are two well-known iterative heuristics that have been applied for solving a range of combinatorial optimization problems in various disciplines of science and engineering [1, 2]. Both of these algorithms have exhibited good performance for the present problem [3, 4]. Therefore, it seems reasonable to hybridize GA and TS with the view of developing an efficient hybrid technique for timing and low power driven placement. A good property of GA is its implicit parallel nature that helps in exploring the search space efficiently. This parallelism is due to the fact that GA processes a population of solutions instead of a single solution. On the other hand, TS showed better results than GA, and this better performance can be attributed to TS searching mechanism. These facts lead us to a proposition that an efficient hybrid technique can be developed by combining the features from these two iterative algorithms.

# References

[1] Sadiq M. Sait and Habib Youssef. VLSI Physical Design Automation: Theory and Practice. *Mc Graw-Hill Book Company, Europe*, 1995.

[2] Sadiq M. Sait and Habib Youssef. *Iterative Computer Algorithms with Applications in Engineering: Solving Combinatorial Optimization Problems.* IEEE Computer Society Press, California, December 1999.

[3] Sadiq M. Sait, Habib Youssef, Aiman Al-Maleh, and Mahmood R. Minhas. Iterative Heuristics for Multiobjective VLSI Standard Cell Placement. *In Proceedings of the INNS-IEEE International Joint Conference on Neural Networks, IJCNN2001*, 3:2224–2229, 2001.

[4] Sadiq M. Sait, Mahmood R. Minhas, and Junaid A. Khan. Performance and low power driven VLSI standard cell placement using Tabu search. *In Proceedings of the IEEE Congress on Evolutionary Computation, CEC'2002.*, 1:372–377, 2002.