QUANTITATIVE ANALYSIS AND COMPUTATIONAL COMPLEXITY OF MEDIA SIGNAL PROCESSING

Aamir A. Farooqui [1], Vojin G. Oklobdzija [2]

1: Synopsys Systems & IP Group, Synopsys® Inc., Mountain View CA 94043-4033, USA
2: Electrical and Computer Engineering Department, University of California, Davis, CA 95616, USA.

Email: aamirf@synopsys.com

ABSTRACT

Media signal processing requires high computing power and the algorithms exhibit a great deal of parallelism on low precision data. The basic components of multi-media objects are usually simple integers with 8, 12, or 16 bits of precision. In order to support efficient processing of media signals, Instructions Set Architecture (ISA) of the traditional processors requires modifications. In this paper, we present the quantitative analysis and the computational complexity required to perform media processing. Main classes of instructions that are needed for the required level of performance of the Media Processor are identified. Their efficient implementation and effect on the processor data-path is discussed. The main operations required in media processing are Addition (with or without saturation), Multiplication (with or without rounding), Sum of Products, and Average of two numbers.

Keywords: *MPEG, VLSI, Computer Arithmetic, Multiplication, IDCT, Datapath.*

الملخص

معالجة إشارات الوسائط يحتاج لطاقة معالجة عالية و لها قابلية عالية للتوازي على البيانات المنخفضة الدقة. الأجزاء الأساسية للوسائط المتعددة تتكون عادة من أعداد صحيحة بدقة ٨،١٢،١٦ بت. ضمان معالجة فعالة لإشارات الوسائط يتطلب تغيير الطراز لجهاز التوجيه (ISA) للمعالجات التقليدية. في هذه الورقة، نقدم التحليل الكمي و التّعقيد الحسابي المطلوب لمعالجة إشارات الوسائط . كما نبين طبقات رئيسية من أوامر التوجية التي نحتاج إليها لحصول على الأداء المطلوب. ونناقش التجربة الفعالة والتأثيرات على أداء ممر البيانات في المعالج. العمليات الرئيسية المضافة هي : الجمع (مع او بدون تشبع)، الضرب (مع او بدون تدوير)، جمع المنتجات، متوسط رقمين.

1. INTRODUCTION

Media signal processing is the real time processing of audio and video signals. Real-time signal processing of audio/video signals is necessary in consumer electronic products, such as personal digital assistants, cellular phones, video games, digital cameras, and high-end communication products, such as IP-telephony gateways, multi-channel modems, speech-processing systems, echo cancellers, image and video processing systems, internet routers, and virtual private network servers. All real-time signal processing algorithms such as,

coding/decoding, and compression / decompression of audio and video signals, are based around certain computation demanding functions such as the Discrete Cosine Transform (DCT), the Inverse Discrete Cosine Transform (IDCT), the Fast Fourier Transform (FFT). These functions are computationally intensive so that special dedicated VLSI circuits or Digital Signal Processors (DSPs) are used in conjunction with the main processor to support these functions

Programmable architectures provide a cost-effective alternative to dedicated VLSI, however, conventional DSP architectures lack the computing power and bandwidth to perform more than one multimedia task at a time. General-purpose microprocessors support media processing by introducing multimedia enhancements in their instruction sets. In these processors a long-word ALU is divided into several small-word ALUs, and several pieces of independent short-word data are processed by a single instruction to perform SIMD operation. This approach was first used for graphics instructions [Intel 1991, K. Deifendorff, et. al., 1992] and gave birth to a new category of processors called Media Processor. A Media processor is defined as programmable processor dedicated to simultaneously accelerate the processing of multiple data types, including digital videos, digital audio, computer arithmetic, text and graphics. Media processors may operate as stand-alone or with a main processor incorporating features such as, peripheral communications interconnect (PCI) interface that actually support their integration onto a PC motherboard [Kuroda, I, et. al., 1998]. They have greater parallelism with lower clock frequencies of 50–200 MHz.

The media processors have an increased processing capability for video, but this multimedia enhancement makes the programming for the microprocessors much more complex. Efficient programming can only be attained if experts tune the software using assembly languages, just as in DSP approaches. There are many MPEG application-specific integrated circuit (ASIC) chips that contain a reduced instruction set computer (RISC) core for control and housekeeping purposes. The most successful approach right now belongs to these classes [M. Harrand, et. al., 1994, T. Arai, et. al., 1997, Makino, H., et. al., 1995, NEC Corporation, 1992]. Most of the major microprocessor architectures have included multimedia instructions in their Instruction Set Architecture (ISA), which supports MPEG-1 and MPEG-2 media standards. The HP PA-RISC was the first ISA to introduce multimedia extension, MAX-1 (Multimedia Acceleration eXtension), in 1994 [Lee. R., 1995]. SUN followed shortly thereafter with the VIS (Visual Instruction Set) in the SPARC ISA [M. Tremblay, et. al., 1998, M. Tremblay, et. al., 1995, S. Rathnam, 1996]. In 1997, HP developed the second generation of MAX-1, called MAX-2, and incorporated it in its 64-bit PA processor [R. B. Lee, 1996]. In the same year, Intel introduced the MMX (Multi-Media eXtension) in its Pentium processor line [A. Peleg, et. al., 1996]. Both SGI and Digital have also announced or introduced multimedia instructions into their respective processor architecture [L. Gwennap, 1996]. Motorola's new AltiVec technology expands the capabilities of PowerPC microprocessors by providing a leading edge, general-purpose processing performance, while concurrently addressing high-bandwidth data

processing and algorithmic-intensive computations in a single-chip solution [Schmookler, M.S., et. al., 1999].

This paper is organized as following: in Section 2 we present the computational complexity and the quantitative estimates to perform block-level MPEG decoding. Section 3 presents the implementation of Add operation and saturated arithmetic for media processing. Overview of different kinds of multiplication operations is presented in Section 4. Finally conclusions are presented in Section 5.

2. QUANTITATIVE ANALYSES OF MPEG DECODING

In this section we present the summary of the quantitative estimates to perform block-level MPEG decoding, detailed analyses can be found in [A. A Farooqui, et. al., 2000]. Based on these estimates we describe new instructions and their implementation to efficiently support media processing. To perform quantitative analysis we made the following assumptions. We assume a bit rate of 4 Mbits/sec from the input bit stream, and the average symbol size is 4 bits, which corresponds to 1 million symbols per second. The frame size is 720 x 480 with 30 frames per second (MP@ML, main profile at main level) in a 4:1:1 YUV format. Therefore each frame contains 8100 (720 x 480 x 1.5), or 243,000, 8x8 micro blocks per second. In this performance analysis it is assumed that the data is already available in the registers (loaded by the main processor or load store unit) and cache hit rate is 100%, and instruction issue rate is one instruction/cycle.

Block-level image processing constitutes the major portion of existing image processing standards, such as H.261 and MPEG-1/2 [M. Berekovic, et. al., 1999, Kuroda, I, et. al., 1998]. Recent MPEG-4 standard offers a much broader range of functionalities and coding modes then the previously defined standards, but still the block-level processing consumes the major portion of MPEG-4 video coding. MPEG decoding requires the following six basic steps:

1. Header Decode.
2. Huffman and Run-length decode.
3. Inverse Quantization.
4. Inverse Discrete Cosine transform.
5. Motion compensation.
6. YUB to RGB conversion.

A summary of the quantitative estimates of the arithmetic operations to perform block-level MPEG MP@ML decoding is presented in Fig. 1. It is clear from these estimates, that the software-only approach to MPEG decoder requires a processing power of 424 MIPS on processors without media enhancement, while SIMD media instructions reduce the MPEG

execution time by approximately three times (143.3 MIPS). The major time consuming operation in MPEG decoding is motion compensation (49.8 MIPS) followed by the display step (41.47 MIPS), and then IDCT (40 MIPS). Fortunately, the two inherently serial steps, decoding the MPEG headers and the Huffman decoding (12 MIPS), are relatively insignificant in execution time [Kuroda, I, et. al., 1998]. The actual MPEG decoder implementation requires a higher processing power due to factors such as cache misses, memory access time, and bus width. However, the number of operations for motion compensation processing is reduced if no pixel interpolation (a non-half-pixel bitstream) is required.

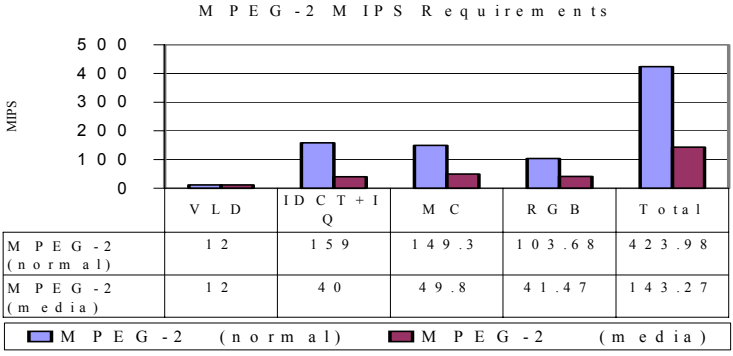

Fig. 1. MPEG-2 MP@ML execution profile with and without media instructions.

Since, the major arithmetic operations in MPEG decoding are addition, and multiplication thus, in order to speed-up the IDCT, motion compensation, and color conversion processing, new instructions have been developed to support these operations. Following we explain the implementation of these instructions considering a 64-bit datapath containing two 64-bit SIMD adders, and 32x32 SIMD multiplier. Fig. 2 shows the macro-level implementation of the two cycle datapath, containing four 16x32 multipliers, 3x2 compressors, and two 64-bit adder-subtractors. This datapath can easily be implemented in VLSI using datapath design tools such as, Synopsys Module Compiler™ [Synopsys Corporation, 2000].

3. ADD/SUB INSTRUCTIONS

The ADD/SUB instructions are executed in the 64-bit partitioned adders of the datapath in the second pipeline stage. Table-1 shows the operation of these instructions on input operands A and B, the result is produced in C and D. The A, B, C, and D can be a byte, half-word, word, or double word packed as 8-bytes, 4-half-words, 2-words, and a double-word respectively; in a 64-bit register Rx, where x = 0…n. The partition of the 64-bit adder is performed according to the partition control signals as shown in Table-2. Since we require two 64-bit adders for the multipliers, therefore by re-using these adders we can support two 64-bit operations in parallel.

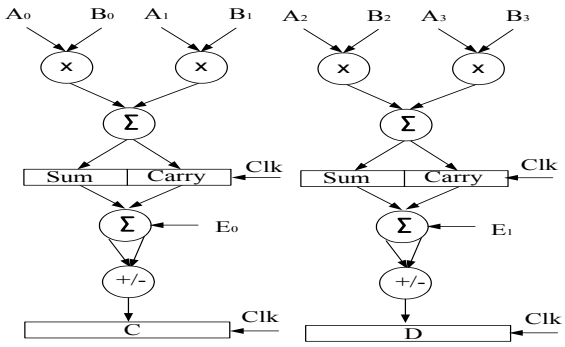

Fig. 2. Macro-level implementation of the datapath.

Table-1. Instructions supported by the ALU (A, B, are the inputs, and C, D are the outputs).

Instruction	Operation	Result
ADD	A + B	C
ADS(U)	A + B	C or SAT(max)
ADS(S)	A + B	C or SAT(min) or SAT(max)
SUB	A-B	C
SUS(U)	A-B	C
SUS(S)	A-B	C or SAT(min) or SAT(max)
BFS(U)	A+B, A-B	C or SAT(max) , D
BFS(S)	A+B, A-B	C, D or SAT(min) or SAT(max)
BFD(U)	(A+B)/2, (A-B)/2	C or SAT(max), D
BFD(S)	(A+B)/2, (A-B)/2	C, D or SAT(min) or SAT(max)
AVG2(U)	(A+B)/2	C
AVG2(S)	(A+B)/2	C

The Add and Subtract operations are performed as normal Addition and Subtraction. The parallel average of two numbers is a very common and useful function in image and video processing: the arithmetic mean as shown in Fig. 3 -a). Only few high performance ISAs [Lee. R., 1995, Schmookler, M.S., et. al., 1999] support this operation. This combined operation involves an addition and a right shift of one bit (divide by two). In the proposed datapath, AVG2 operation is implemented using the 64-bit partitioned adder; performing normal addition and finally shifting the result one bit right. The datapath shifts in the carry out bit as the most significant bit of the result, so it has the added advantage that no overflow can occur.

3.1. Butterfly

Butterfly is an important operation, which is frequently required in FFT, and IDCT. Butterfly operation is performed as shown in Fig. 3 -b). In the proposed datapath the Butterfly (BFS) and Butterfly Divide by 2 (BFD) instructions are implemented using the two 64-bit partitioned adders. In this operation one 64-bit adder performs the addition while the other one performs the subtraction in parallel, at the end two results are combined to produce the final result.

Table-2. Partition of the ALU, using Partition control signals.

Part1Part0	ALU partition
00	Byte
01	Half_word
10	Word
11	Double_word

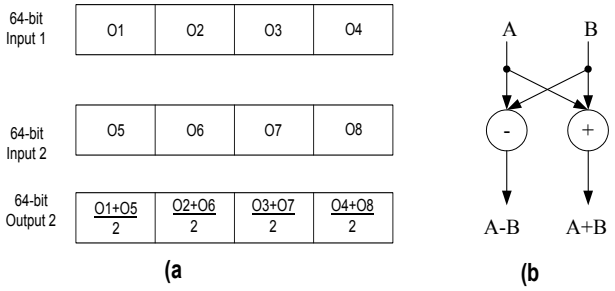

Fig. 3. a) Parallel averaging operation, b) Butterfly Operation on A and B.

The BFD instruction performs the addition and subtraction of two operands simultaneously and then divides the result by two (shift right). Since, we are performing AVG2 operation, therefore the BFD operation is performed using the same circuit. There are two types of BFD instructions one is for signed operands; the other is for unsigned operands. The basic operation for both the instructions is the same, but in case of signed operands, the sign of the result is extended during the shift right operation.

3.2. Saturated Arithmetic

In multimedia arithmetic we deal mostly with 8 or 16-bit pixel data, the data represent the color intensity and luminous information. To represent this data we cannot use modulo arithmetic in which the overflow is ignored, because a small change in color intensity or luminous may result a huge a change in the resulting information, for e.g., from FFHex to 00Hex (white to

black). Therefore, in media signal processing we use saturated arithmetic. In case of saturated arithmetic it is necessary to clamp overflowing results to a high or low value.

There are two modes of saturation asymmetric and symmetric. For unsigned integers, the two modes are the same. While, for signed values, symmetric mode saturates positive and negative numbers to the same absolute value function, for instance signed byte saturation values of -127 and +127. The asymmetric mode will saturate the negative value to a number, which is an absolute value of one greater than the positive value, for instance -128 and +127 for sign bytes. The proposed datapath can support only asymmetric mode of saturation. The conditions for saturation resolution based on overflow/underflow are summarized in Table-3 and Table-4, for Add and Subtract operations respectively. In these tables, A and B are the input operands and As, and Bs, are the sign bits of these operands. In case of unsigned addition an overflow occurs when carry out is '1' and the result is saturated to the maximum value. While, in case of unsigned subtraction an underflow occurs when carry out (C_{out}) is '0' and the result is saturated to the minimum value. Similarly, in the case of signed addition an overflow occurs when both the input operands are positive and carry out and carry out-1 (C_{out-1}) are '1'. In this case, the result is saturated to the maximum positive value. These rules are summarized in Table-3 and Table-4.

Table-3. Overflow and underflow detection for Add operation.

Data type	MSB	Operation	Overflow	Underflow
Unsigned		A + B	$C_{out} = 1$	
Signed	As=0, Bs = 0	A + B	$C_{out}XORC_{out-1}$	
	As=1, Bs = 1	A + B		$C_{out}XORC_{out-1}$
	As=1, Bs = 0	A + B		
	As=0, Bs = 1	A + B		

Table-4. Overflow and underflow detection for Subtract operation.

Data type		Operation	Overflow	Underflow
Unsign		A - B		$C_{out}= 0$ (A<B)
Sign	As=0, Bs=0	A - B		
	As=1, Bs=1	A - B		
	As=1, Bs=0	A - B		$C_{out}XORC_{out-1}$
	As=0, Bs=1	A - B	$C_{out}XORC_{out-1}$	

4. MULTIPLY INSTRUCTIONS

Multiplication is one of the most important operations in digital signal processing. Media processing requires different kinds of multiply, and multiply with accumulate operations on signed and unsigned operands, with or without rounding of the result. Fig. 4 shows the multiply and multiply accumulate instructions required for the efficient processing of media signals. These instructions are executed using 32x16 multiplier blocks of the datapath. The input operands are A and B, the result is produced in C and D. A and B can be a byte, half-word, 24-bit or word packed as 8-bytes, 4-half-words, 2-24-bit or 2-words in a 64-bit register Rx, where x = 0…n. The partition of the multipliers is performed according to the partition control signals as shown in Table-2 for the ALU. The only difference is that '11' is used for 24-bit operation instead of 64-bit operation. The multiplier hardware is configured for signed and unsigned operation using the sign control bit. When 'Sign' bit is '1' signed multiplication is performed and when it is '0' unsigned multiplication is performed. All the multiplication instructions require two-cycle latency with a single-cycle throughput.

4.1. Multiply

The MUL operations are performed as normal multiplication. In simple multiply operation, the two input operands are multiplied in the first cycle producing Sum, and Carry vectors. In the second cycle sum and carry vectors of AxB are added using the 64-bit partitioned adder to produce the final result as shown in Fig. 4. Since the result of multiplication is twice the width of the input operands, the result of simple multiplication is produced in C and D (C contains the lower half of the result and D contains the upper half of the multiplication). The only difference in MUL (U) and MUL(S), is that MUL(U) is the unsigned multiplication, while MUL(S) is the signed multiplication. Fig. 4-a) shows the datapath for 8x8 and 16x16 multiplication. Fig. 4-b) shows the datapath for 24x24 and 32x32 multiplication, which requires two 16x32 multipliers.

Table 5. Multiply operations supported by the proposed datapath.

Instruction	Mnemonic	Operation
Multiplication with full resolution	MUL (S/U)	C = A*B
Multiplication with accumulate	MULA(S/U)	C = A*B + C'
Multiplication with deduct	MULD(S/U)	C = A*B - C'
Multiply upper half result with rounding	MULH(S/U)	C = A_h*B_h
Sum of two products	SUMP (S/U)	A_1*B_1 + A_0*B_0
Sum of two products with accumulate	SUMPA (S/U)	A_1*B_1 + A_0*B_0 + C'
Sum of two products with deduct	SUMPD (S/U)	A_1*B_1 + A_0*B_0 - C'

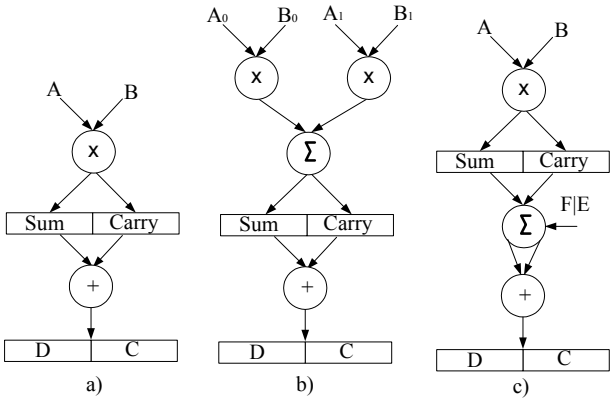

Fig. 4. Two cycle multiply operation a) 8x8 or 16x16, and b) 24x24 or 32x32, and c) multiply accumulate operation.

4.2. Multiply Accumulate Operation

In the case of the multiply accumulate operation (MULA), the two input operands are multiplied in the first cycle producing Sum and carry vectors, then a third operand F|E (F concatenated to E) is added with the Sum and carry vectors of AxB in the second cycle using the 4x2 compressor. The output of the 4x2 compressor is finally added using the 64-bit partitioned adder to produce the final result as shown in Fig. 4-c).

4.3. Sump

Sum of two products is an important operation supported by most of the high performance media processors. This operation performs the addition of two products and it is equivalent to two multiply and one addition as shown below:

$C = A_0xB_0 + A_1xB_1$

The proposed datapath performs the addition of two products (SUMP instruction) in two cycles with single cycle throughput. The instruction execution at macro level is shown in Fig. 5. This instruction requires two multiplications A_1xB_1, and A_0xB_0. These multiplications are performed in the first cycle using the MUL 32x16 blocks. In case of byte and half-word operation the summation of two products is performed in the first cycle (Fig. 5-a) using the 4x2 compressor after the multipliers. While in case of word operation, first cycle 4x2 compressor is used for the addition of the partial products of the 32x32 multiplication. Therefore, the summation of two 32x32 products is performed in the second cycle (Fig. 5-b) using the second 4x2 compressor. The sum and carry vectors produced by the summations are finally added

using the 64-bit partitioned adder to produce the addition ($A_1xB_1+ A_0xB_0$) as shown in Fig. 5. In order to produce the result of the same bit width as the input the result of the addition is rounded and only the upper half of the result is stored in the output.

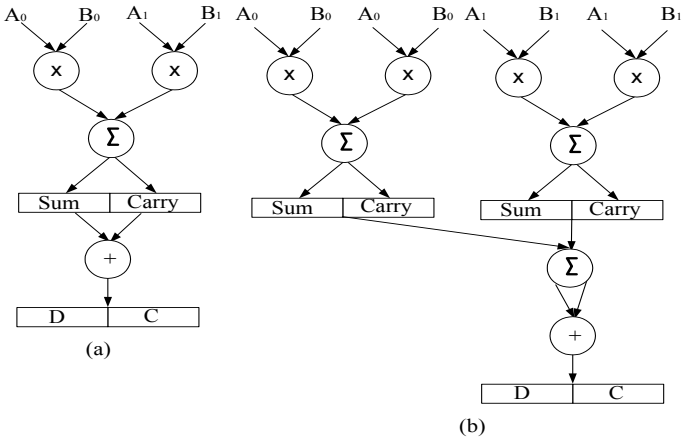

Fig. 5. Sum of two products: (a) Byte or half-word, and (b) 32x32.

5. CONCLUSION

In this paper, we present the quantitative analysis and the computational complexity required to perform media processing. It is clear from these estimates, that the software-only approach to MPEG decoder requires a processing power of 424 MIPS on processors without media enhancement, while SIMD media instructions reduce the MPEG execution time by approximately three times (143.3 MIPS). The major time consuming operation in MPEG decoding is motion compensation (49.8 MIPS) followed by the display step (41.47 MIPS), and then IDCT (40 MIPS). Fortunately, the two inherently serial steps, decoding the MPEG headers and the Huffman decoding (12 MIPS), are relatively insignificant in execution time. The actual MPEG decoder implementation requires a higher processing power due to factors such as cache misses, memory access time, and bus width. However, the number of operations for motion compensation processing is reduced if no pixel interpolation (a non-half-pixel bitstream) is required. Based on these estimates main classes of instructions that are needed for the required level of performance of the Media Processor are identified. Their efficient implementation and effect on the processor data-path is discussed. The main operations required in media processing are Addition (with or without saturation), Multiplication (with or without rounding), Sum of Products, and Average of two numbers.

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Top