A Crystal-Tolerant Fully Integrated Frequency Synthesizer For GPS Receivers:System Perspective

Tarek Elesseily
LSI Logic FZE
Dubai, U.A.E
Email: tarek.elesseily@lsi.com

Khaled M. Sharaf
Integrated Circuits Laboratory
Ain Shams University
Cairo, Egypt
Email: kmsharaf@ieee.org

***Abstract*— This paper presents the system level design of a frequency synthesizer for dual band GPS receivers that can be easily integrated in wireless phones (mainly GSM mobile phones). For the ease of integration with GSM wireless systems the synthesizer can tolerate most of the common GSM crystals, besides the GPS crystals.**

The presented synthesizer was designed to target a low IF down conversion receiver with a tolerable IF range of 10% around 4.092MHz which allows the use of the famous 10/13/26MHz GSM crystals and all the GPS crystals. The designed frequency synthesizer generates the LO signals for both L1/L2 bands (1.5713GHz/1.2317GHz) with an average phase noise of -95dBc/Hz,consuming 4.05mW/4.5mW for L1/L2 respectively at 1.2V supply.

I. Introduction

The fundamental Global Positioning System (GPS) technique intends to get accurate positions, velocity, and time data by using one-way ranging signal from the satellites. It is being widely used in car navigation systems, auto-vehicle location systems, intelligent transport systems, and so on.The GPS ranging signal broadcasting from the satellites uses two frequencies: a primary signal at 1575.42MHz (LI band) and a secondary signal at 1227.6MHz (L2 band).

The L1 signal from each satellite is modulated by two pseudo random codes, the coarse acquisition (C/A) code and the precision (P) code. The P-code is normally encrypted, with the encrypted version of the P-code referred to as the Y-code. The L2 signal is modulated by the new civil signal (C/S) code and the P-code. Ll/L2 dual-band receivers have the ability to make ionospheric delay calculations from the fact that the propagation speed of L1 and L2 differ with varying ionospheric conditions.

One of the main drawbacks of the current GPS system is its poor sensitivity in a multi-path environment. To overcome this limitation, the GPS modernization plan added a new civil code called C/S on L2 band.The primary need of L2 C/S was to eliminate the unacceptable 21-dB cross-correlation performance of the C/A code, which allows a strong GPS signal to interfere with weak GPS signals. The L2 C/S signal achieves this by having a worst-case cross-correlation performance of 45 dB, allowing a better indoor signal reception which makes the integration of GPS receiver in wireless phones possible [1], [2].

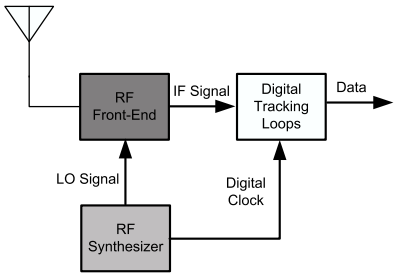

Fig. 1. Basic GPS System Components

The GPS receiver system, consists of three main parts:RF Front End, Digital demodulation loop, and finally the frequency synthesizer. Figure 1 elaborates the GPS receiver basic components.

The frequency synthesizer supplies both the RF Front End and the digital parts with two different frequencies. A new frequency plan will be introduced in II.

The paper is divided in to three sections, Introduction and then description of the frequency plan followed by the system level design and block specifications.

II. Frequency Plan

The frequency plan for the the GPS system shown in Figure2 targets: 1) L1/L2 Dual band operation,2) Operation with GSM common crystals,3) Operation with all GPS crystals,4) IQ output from the LO ,5) Satisfies the complex filter IF frequency tolerance, and 6) Deliver a digital clock for the demodulation part.

A. Front-End Clock Generation

In this section, the values of the Reference (R),Feedback (N) dividers, Intermediate Frequency (IF) and VCO frequency range are going to be evaluated according to the above constraints. Some facts had to be taken into consideration (1) before evaluation.

$$f_o = 1.0230MHz \quad (1)$$

$$IF = Xf_o \quad (2)$$

$$F_{xtal} = Yf_o \quad (3)$$

$$L1 = 1540f_o \quad (4)$$

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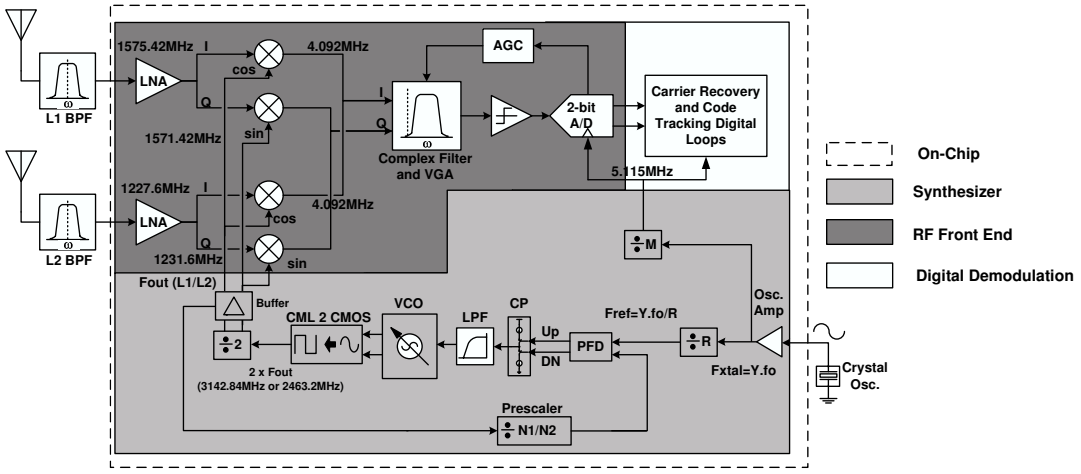

Fig. 2. GPS System Components

$$L2 = 1200 f_o \tag{5}$$

Where;X, Y are integer numbers, L1, L2 are the two GPS bands and F_{xtal} is the crystal frequency.

To satisfy above targets and considerations equation (6) has to be solved and all its possible solutions are to be evaluated.

$$X f_o = |L1 \pm N1Y f_o| = |N2Y f_o \pm L2| \tag{6}$$

Where $X f_o$ is the intermediate frequency (IF), N1 is the L1 band PLL division factor,N2 is the L2 band PLL division factor, and $Y f_o$ is the crystal frequency.

$$Y f_o N_{total} = L1 + L2 = Y f_o(N2 + N1) \tag{7}$$

Where; $N_{total} = N2 + N1$

The (IF) frequency choice is dependent on equation (6) and other system constraints, that can be summarized in the following

- To be chosen away from the flicker corner i.e $\geq 2MHz$
- To decrease power consumption it should be minimized i.e $\leq 10MHz$
- To facilitate complex filter design it's preferable to decrease the IF frequency

From the above mentioned constraints the X value is chosen to be in the range from 4 to 6. Solving equation(6), using equation (1), $X = [4 : 6]$ and $Y = [1 : 20]$. Bearing in mind that a GPS originated crystals are being used, four possible sets of solutions are found

1) Set One,Set Two and Set Three: Set one solutions are evaluated from equation (8), this equation elaborates that both frequencies $N1Y f_o$ and $N2Y f_o$ are inside the frequency range between L1 and L2.

$$X f_o = L1 - N1Y f_o = N2Y f_o - L2 \tag{8}$$

Y	Ntotal	N1 Range	N1(X value) possible solutions
1	2740	$1534 \leq N1 \leq 1536$	1534(6),1535(5),1536(4)
2	1370	$767 \leq N1 \leq 768$	767(6),768(4)
4	685	$383.5 \leq N1 \leq 384$	384(4)
5	548	$306.8 \leq N1 \leq 307.2$	307(5)

TABLE I
SET ONE ACCEPTABLE SOLUTIONS

$$Ntotal = N1 + N2 = L1 + L2 = 2740 f_o \ , atY = 1 \tag{9}$$

Table I shows all possible acceptable solutions for set one. For set Two,equation (10) shows that the frequency $N1Y f_o$ is above L1 band and $N2Y f_o$ is inside the frequency range between L1 and L2. Set Two solutions are exactly the same as Set One.The same is applicable for set three having evaluated from equation (12), this equation shows that the frequency $N1Y f_o$ is above L1 band and $N2Y f_o$ is below L2 band.

$$X f_o = L1 + N1Y f_o = N2Y f_o - L2 \tag{10}$$

$$Ntotal = -N1 + N2 = L1 + L2 = 2740 f_o \ , atY = 1 \tag{11}$$

$$X f_o = L1 + N1Y f_o = N2Y f_o + L2 \tag{12}$$

2) Set Four:
Set Four solutions are evaluated from equation (13), this equation shows that the frequency $N2Y f_o$ is below L2 band and $N1Y f_o$ is inside the frequency range between L1 and L2.

$$X f_o = L1 - N1Y f_o = N2Y f_o + L2 \tag{13}$$

$$Ntotal = N1 + N2 = L1 - L2 = 340 f_o \ , atY = 1 \tag{14}$$

The solution for (13), will give N1 range to be always greater than Ntotal, so no possible solutions are found in this range.

Considering the four solutions, the first three are giving redundant solution which is set one and the fourth gives no solution. All possible solutions for GPS crystals can be summarized in table II. The selection criteria is based on using the minimum division factors needed, leading to the choice of rows 3 and 5 in table II. Two possible IF frequencies are now available $4 f_o and 5 f_o$.

A second dimension in our selection criteria is to guarantee the correct operation of most common GSM crystals.TableIII and tableIV show the different division factors for both feedback dividers (N) and Reference divider (R).The receiver complex filter can withstand a tolerance of 10% in the IF frequency as described in [3], [4]. From the tables III and IV we can see that using the IF frequency 5.115MHz won't be acceptable from the complex filter tolerance point of view as both the 13MHz and 26MHz did not pass for variation $\leq$ 10%.On the other hand using the IF frequency 4.092MHz can overcome this specification using certain reference division factors. From this a conclusion can be taken to use the 4.092MHz as an IF frequency.

B. Digital Clock

The digital clock can be generated as seen in figure2 through the (M) Divider , that is directly connected to the oscillator amplifier. The digital clock is designed to be in the 5MHz frequency range with tolerance of about 20 %. The maximum needed division factor happens while using the 26MHz GSM crystal and $40 f_o$ GPS crystal. This implies that the maximum division factor is approximately $\frac{40}{5}$ that gives 8.

III. PLL System Level Design

A. System Overview

The synthesizer shown in figure 2 is used to supply both the RF Mixer and the demodulation digital loop by two different clocks as mentioned in section II. An Integer-N synthesizer type is chosen to satisfy the system requirements.

The whole system is designed to be integrated including the VCO and Loop Filter. The RF Mixer requires a quadrature differential output from the synthesizer. This can be done by designing the VCO at double its frequency then use a divide by two circuit to obtain the I/Q output required. The VCO is designed to cover both L1/L2 frequency ranges, an LC VCO is preferred than other architectures due to power consumption. A pulse swallow divider is used to cover the needed division factors according to the frequency plan. A programmable reference divider is also used to guarantee the multi crystal operation. A third order loop filter is used to suppress the spurs more than 65dB from carrier. A programmable charge pump is used to ensure loop stability as the division factor changes.

Crystal	N	R	Fref	BW	Φ_m	I_{CHP}	O/p Freq
16fo	301	4	4.092M	40K	59	50u	1.23GHz
16fo	384	4	4.092M	40K	59	64u	1.57GHz
4fo	301	1	4.092M	40K	59	50u	1.23GHz
4fo	384	1	4.092M	40K	59	64u	1.57GHz
5fo	241	1	5.115M	80K	59	40u	1.23GHz
5fo	307	1	5.115M	50K	60	51u	1.57GHz
10M	985	8	1.250M	12.5K	60	164u	1.23GHz
10M	1257	8	1.250M	44K	55	220u	1.57GHz
13M	753	8	1.625M	16K	55	125u	1.22GHz
13M	972	8	1.625M	16K	55	161u	1.57GHz
26M	753	16	1.625M	16K	55	125u	1.22GHz
26M	972	16	1.625M	16K	55	161u	1.57GHz

TABLE V
GPS/GSM Crystals Vs. Loop parameters and frequency Division factors

B. System Design

The system design is based on some design aspects [5], [6], that can be summarized in:Having minimum phase shift at unity gain frequency of the loop to ensure loop stability, Phase Margin is chosen between 30 and 70 Degrees (60 degrees), Loop bandwidth is chosen 1/100 from the reference frequency (approximately 50KHz) and finally to increase the spur level attenuation a 3rd order loop filter is used.

To ensure loop stability all over the division ranges the charge pump current and loop bandwidth are changing as the division factor changes.

Table V summarizes the Loop parameters, output frequency, charge pump current,loop bandwidth and division factors for N and R at all crystal frequencies.The VCO gain is approximately 50MHz/Volt.

C. Noise Requirements

The phase noise of a local oscillator corrupts the spectrum and degrades the (C/N_o).

Multiplication in the time domain corresponds to convolution in the frequency domain, and hence the added noise density due to the phase noise is calculated by [1]:

$$\begin{aligned} N_{PN}(\omega) &= N_{IN}(\omega) * S_{LO}(\omega) \\ &= \int_{-\infty}^{\infty} N_{IN}(\omega) S_{LO}(\omega - \omega') d\omega' \\ &= N_o \int_{-\infty}^{\infty} S_{LO}(\omega) d\omega \end{aligned} \tag{15}$$

where $S_{LO}(\omega)$ is the phase noise of an LO. The last integral term is equivalent to the absolute rms jitter of the oscillator, normalized to its period, thus,

$$\left(\frac{N_{PN}}{N_o}\right) = \int_{-\infty}^{\infty} S_{LO}(\omega) d\omega \approx \left(\frac{\Delta T_{LO_{rms}}}{T_{LO}}\right)^2 \equiv (\sigma_{rms}^2) \tag{16}$$

Y	Crystal	N1	N2	Fout (L1)	Fout (L2)	X	IF
1	1.023MHz	1536	1204	1.5713GHz	1.2317GHz	4	4.092MHz
2	2.046MHz	768	602	1.5713GHz	1.2317GHz	4	4.092MHz
4	4.092MHz	384	301	1.5713GHz	1.2317GHz	4	4.092MHz
1	1.023MHz	1535	1205	1.5703GHz	1.2327GHz	5	5.115MHz
5	5.115MHz	307	241	1.5703GHz	1.2327GHz	5	5.115MHz
1	1.023MHz	1534	1206	1.5693GHz	1.2337GHz	6	6.138MHz
2	2.046MHz	767	603	1.5693GHz	1.2337GHz	6	6.138MHz

TABLE II

GPS CRYSTALS POSSIBLE DIVISIONS FOR DUAL BAND OPERATION

Crystal	R	Fref	N1	N2	F(N1)	F(N2)	IF(N1)	Var.	IF(N2)	Var.
10MHz	2	5.MHz	314	247	1.57GHz	1.2350GHz	5.42MHz	5.9	7.4MHz	-44.6
10MHz	4	2.5MHz	628	493	1.57GHz	1.2325GHz	5.42MHz	-5.9	4.9MHz	4.2
13MHz	2	6.5MHz	243	188	1.5795GHz	1.2220GHz	4.08MHz	20.2	5.6MHz	9.4
13MHz	8	1.63MHz	973	752	1.5811GHz	1.2220GHz	5.705MHz	-11.5	5.6MHz	9.4
26MHz	4	6.5MHz	243	188	1.5795GHz	1.2220GHz	4.08MHz	20.2	5.6MHz	9.4
26MHz	16	1.63MHz	973	752	1.5811GHz	1.2220GHz	5.705MHz	-11.5	5.6MHz	9.4

TABLE III

GPS CRYSTALS AND IF FREQUENCY VARIATION FROM 5.115MHZ

Crystal	R	Fref	N1	N2	F(N1)	F(N2)	IF(N1)	Var.	IF(N2)	Var.
10MHz	2	5MHz	314	246	1.57GHz	1.23GHz	5.42MHz	32.4	2.4MHz	41.3
10MHz	8	1.25MHz	1257	985	1.57GHz	1.23GHz	4.17MHz	1.9	3.65MHz	10.08
13MHz	2	6.5MHz	243	188	1.57GHz	1.22GHz	4.08MHz	0.2	5.60MHz	36.8
13MHz	8	1.63MHz	972	753	1.57GHz	1.22GHz	4.08MHz	0.2	3.97MHz	-2.8
26MHz	4	6.5MHz	243	188	1.57GHz	1.22GHz	4.08MHz	0.2	5.60MHz	36.8
26MHz	16	1.63MHz	972	753	1.57GHz	1.22GHz	4.08MHz	0.2	3.97MHz	-2.8

TABLE IV

GPS CRYSTALS AND IF FREQUENCY VARIATION FROM 4.092MHZ

The effective C/N_oat the mixer output can be written by:

$$\left(\frac{C}{N_o}\right)_{\text{OUT}} = \left(\frac{C}{N_o + N_{\text{PN}}}\right) = \left(\frac{C}{N_o}\right)_{\text{IN}} \times \left(\frac{1}{1+\sigma_{rms}^2}\right) \quad (17)$$

To obtain less than 0.1-dB loss [3], the averaged phase noise should be lower than -80 dBc/Hz.

D. Synthesizer Blocks Specifications

Table VI shows the summary of block specifications

Block	Noise	Max Freq.	Programmability
Osc. amplifier	-140dBc/Hz	50MHz	N.A.
R Divider	-160dBc/Hz	50MHz	4-bit synchronous counter
M Divider	-160dBc/Hz		4-bit synchronous counter
PFD/CHP	8pA/$\sqrt{Hz}$	50MHz	5-bit current control
VCO	-110dBc/Hz 1MHz	3.2GHz	2-bit fine, 1-bit coarse tuning
CML2CMOS	-125dBc/Hz 1MHz	4GHz	N.A.
Div2	-160dBc/Hz	4GHz	N.A.
Feedback Divider	-160dBc/Hz	4GHz	4 & 7 bit counters

TABLE VI

SYNTHESIZER BLOCKS SPECIFICATIONS

IV. CONCLUSION

In this paper, the Synthesizer system level design is presented for an L1/L2 dual band GPS receiver. The frequency plan and all Synthesizer blocks specifications are introduced. The designed frequency synthesizer generates the LO signals for both L1/L2 bands (1.5713GHz/1.2317GHz) with an average phase noise of -95dBc/Hz,consuming 4.05mW/4.5mW for L1/L2 respectively at 1.2V supply.

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