Artificial Neural Network Based Modeling of GaAs HBT and Power Amplifier Design for Wireless Communication System

M. S. Alam
Department of Electronics Engineering, Z.H. College of Engineering & Technology
A.M.U. Aligarh 202002 India
Email: m.alam@ee.qub.ac.uk

O. Farooq
Department of Electronics Engineering
A.M.U. Aligarh 202002 India

Izharuddin
Department of Electronics Engineering
A.M.U. Aligarh 202002 India

G.A. Armstrong
School of Electrical & Electronics Engineering Queen's University of Belfast
BT9 5AH UK

***Abstract*— The power amplifier (PA) used in modern wireless system needs to perform better from point of view linearity and efficiency. A crucial perquisite for the design of PA is the availability of suitable device models. Artificial neural networks (ANN) recently gained attention as a fast and flexible way to develop HBT device model when compared to the conventional modeling approach based on empirical equations and can demonstrate better accuracy. The framework for this ANN based model is a common-emitter large-signal equivalent circuit model, which has been implemented in Agilent Advance Design System (ADS) simulation environment. An excellent agreement between modeled and bias dependent DC and S -parameters and harmonic power in non-linear mode of operation was obtained. Using developed ANN based HBT model PA design was carried out. At collector voltage V_c of 3.4V, the power amplifier shows an excellent linearity (first ACPR<-42.2dBc) up to 28dBm of rated output power for CDMA applications. At the rated output power level, PAE was found to be more than 35%. All the CDMA wireless PA specifications like gain, power-added efficiency (PAE) and adjacent channel power rejection (ACPR) are achieved over nominal and extreme temperature conditions.**

Index Terms— Neural Network, Power Amplifier, GaAs HBT, Large Signal Modeling, Equivalent Circuit Model

I. Introduction

In recent years, there has been a high demand for hetero-junction bipolar transistors (HBTs) for design of PA used in wireless due to their better linearity superior high-frequency performance [1]-[2]. For the design of nonlinear circuits such as power amplifiers, a nonlinear model needs to be developed. The most common models for HBTs are compact models such as GP [3], HICUM [4], MEXTRAM [5], and VBIC [6]. The general drawback of these compact models is that well calibrated data from an appropriate foundry may not always be readily available.

Artificial neural networks (ANNs) have been in use to replace empirical equations or compact models for a variety of devices such as HEMT [7], MESFET [8], CMOS [9,10] and HBT [11]. These models are based on an equivalent circuit and require less time for their development compared to compact models and offers many advantages:

i) ANN based models are universal function approximators [12] and allow reuses of the same modeling technology for both linear and non-linear problems at both device and circuit levels.

ii) Neural networks can "learn" from measured device data, allowing model development, even when formulae are unavailable.

iii) ANN based model is simple to extract, easy to build and fast to evaluate.

The equivalent circuit model based on ANN has been used to carry out non-linear modeling of HBT [13]. However in application of [13] there are a number of difficulties. For example, equivalent circuit model parameters extraction relies on specially designed test structures and numerical optimizations, which may even lead to unphysical parameter values. In addition the non-linearity of a single element such as base-emitter capacitance C_{be} is accounted for, while the remaining intrinsic parameters are treated as bias independent.

Using our approach of analytical parameter extraction [14] at number of bias points, it has been found that intrinsic parameters show their expected dependency on bias (i.e. different base voltage V_b and collector voltage V_c), while extrinsic parameters have been found to be virtually independent of bias. Bias dependency of critical intrinsic elements, while not considered in [13], is in fact essential in order to improve model accuracy.

In this work, a two-layered neural network architecture (4 neurons in first layer and 1 neuron in second layer) is used to model each intrinsic parameter. A comparative study of two-layered and three-layered architecture [9,10] (2-neurons in first layer and 2-neurons in second layer and 1 neuron in third layer) for various intrinsic HBT parameters shown in Fig. 1 has been carried out. It has been found that the performance of two-layered architecture is superior as evident from results of C_{be} shown in Fig. 2. Similar better performances from two-layered architecture were obtained for rest of intrinsic parameter shown in Fig.1.

The trained ANN weights are used to develop bias dependency function for intrinsic parameters. The model has

1-4244-0765-6/06/$20.00 ©2006 IEEE

been implemented in Agilent ADS [15] simulation environment and excellent agreement is obtained when compared with the measured results of bias dependent DC and S-parameters (0.25-26.5GHz). More significantly the capability of the ANN based model in predicting harmonic distortion is significantly much better than a traditional HBT SPICE model as shown in Fig. 3.

II. Design of Power Amplifier

The GaAs HBT power amplifier circuit shown in Fig. 4 and developed to operate in the frequency range between 1-2 GHz ranges. It consists of 2 stages of amplification. The first stage has a 10 transistors (unit cells) in parallel and second stage has 36 transistors (unit cells) in parallel. The first and the second stage base dc supply voltages are V_{B1} and V_{B2} respectively, which are derived from a temperature compensated bias control circuit as shown in Fig. 4. The bias circuit has been designed carefully, so that bias current increases linearly with temperature over range –20 ^{0}C to +80 ^{0}C in order to maintain constant power gain over the full temperature range. The V_{C1} and V_{C2} typically 3.4 V are, respectively, the first and second stage battery collector supply voltages. V_{REF} typically 3 V provides a precisely controlled regulated supply to accurately define bias current. V_{CONT} determines the mode of operation of PA, which is a function of bias current (V_{CONT} = 0V; high mode of operation and V_{CONT} = 3 V; low mode of operation). The number of cells in each stage of the amplifier is chosen to distribute the gain between the 2 stages, so that the maximum recommended current density of the individual transistors (unit cell) is not exceeded. The PA includes feedback arrangement in both first and second stage as shown in Fig. 4, which is known to have large impact on stability. The ANN based non-linear model of unit cell of size $2\times3\times30\mu m^2$ is multiplied by 10 and 36, respectively to replace 1st and 2nd stage transistors shown in Fig. 1and PA simulations are carried out as discussed in next section.

III. Simulation Results

The PA module shown in Fig. 4 will be assessed to evaluate performance measures like gain, linearity and power added efficiency (PAE) under CDMA excitation at different temperatures.

Fig. 5 shows the simulated result of bias current over the temperature range –20^{0}C to 85^{0}C when the value of V_{REF} = 2.9 V under low mode of operation. It can be observed that the bias collector current, I_C monotonically increases with increase in temperature. Similar results were obtained under high mode of operation. The increase in I_C compensates for the roll-off in dc-current gain β with increase in temperature. Thus, making gain of the HBT PA amplifier stable even under extreme temperature conditions.

The graph of Fig. 6 shows the behavior of PA under low mode (V_{CONT} = 3 V) of operation. The amplifier gain, ACPR and PAE are shown for 1880 MHz PCS band. The curves show that amplifier gain lies within ± 0.85dB up to 28 dBm output power at various temperature condition, while a typical ACPR spec of –42.2 dBc and PAE >35% of wireless system for PA are achieved [16].

The temperature is nominally taken to be 25^{0}C for simulation. The simulations show the performance measure at some extreme temperature such as –20 ^{0}C, and 80 ^{0}C. Similarly, in high mode of operation gain variation is in the range of ± 1 dB up to 28dBm output power at various temperature conditions. The gain achieved in higher mode is more than low mode of operation, which could be due to large variation in bias current in high mode operation compared to low mode.

IV. Conclusions

We have reported a neural network based non-linear model for GaAs HBT. Bias dependent intrinsic parameter variation is difficult to formulate accurately using empirical equations. Therefore, we have used simple 2-layered neural network architecture to implement parameter bias dependence of critical intrinsic parameters of GaAs HBT. The non-linear mode of operation of the neural network model has been validated including harmonic power and good fits were obtained under large signal operation. Under such conditions the predictive capability of the ANN based model in modeling harmonic distortion is significantly better than a traditional GaAs HBT SPICE model.

The design PA circuit is verified through the simulation of various performances like gain, ACPR and PAE at different temperatures. The PA operates over range of temperatures whilst maintaining credible performance. The results establish the GaAs HBT PA superiority for modern 3G wireless systems as compared to other technology.

References

[1] A. Shirvani, D. Su, and B.A. Wooley, "A CMOS RF Power Amplifier with Parallel Amplification for Efficient Power Control," *IEEE Journal of Solid State Circuits,* vol. 37, pp. 684-693, 2002.

[2] M.S. Alam, "RF Modelling of deep sub-micron CMOS and heterojunction bipolar transistor for wireless communication systems," *Ph.D. dissertation, School of Electronic and Electrical Engineering, Queen's University of Belfast (UK), 2002*

[3] H. K. Gummel and H. C. Poon, "An integrated charge control model of bipolar transistors," *Bell System Technology Journal*, vol. 49, pp. 827-852, 1970.

[4] M. Schroeter, S. Lehmann, H. Jiang and S. Komarow, "HICUM/Level 0-A simplified compact bipolar transistor model," *In Proc. IEEE Bipolar/BiCMOS Circuits Technology Meeting*, 2002, pp. 112-115.

[5] W. J. Kloosterman, J. A. M Geelen, and D. B. M. Klassen, "Efficient parameter extraction for the MAXTERM model," *In Proc. IEEE Bipolar/BiCMOS Circuits Technology Meeting*, 1995, pp. 70-73.

[6] K. Lee, K. Choi, S. H. Kook, D. H. Cho, K.W. Park, and B. Kim, "Direct Parameter Extraction of SiGe HBTs for the VBIC Bipolar Compact Model," *IEEE Transaction on Electron Devices*, vol. 37, pp. 375-385, 2005.

[7] K.Shirawawa, M. Shimizu, N. Okubo, and Y. Daido, "Structural Determination of Multi-layered Large-Signal Neural Network HEMT Model," *IEEE Trans. Microwave Theory and Techniques*, vol. 46, pp. 1367-1375, 1998.

[8] A. H. Zaabad, Q. J. Zhang, and M. S. Nakhla, "Neural Network Modelling Approach to Circuit Optimization and Stastical Design," *IEEE Transaction On MTT*, vol. 43, pp. 1349-1358, 1995.

Top

[9] B. Toner, M. S. Alam, V.F Fusco and G. A. Armstrong, "Neural Network Based Time Domain Modelling of 0.18um MOSFETs," *Microwave Optical Technology Letters (U.S.A)*, vol. 35, pp. 203-206, 2002

[10] M. S. Alam, G. A. Armstrong, B. Toner and V. F. Fusco, "Non-linear Modeling of 0.18 µm CMOS using Neural Networks," *Microwave Optical Technology Letters (U.S.A.)*, vol. 37, pp. 53-56, 2003.

[11] V. K. Devabhaktuni, X. Xi, and Q. J. Zhang, "A neural network approach to modeling of heterojunction bipolar transistors from S-parameter data," *In Proc. 28th European Microwave Conference*, Amsterdam, Netherlands, pp. 306-311, 1998.

[12] K. Hornik, "Multi-Layered Feed-forward Neural Networks are Universal Approximator," *Neural Networks*, vol. 2, pp. 259-266, 1990.

[13] H. Taher, D. Schreurs, E. Vestiel, and R.Gillon, "Nonlinear Modelling of Si/SiGe HBT Using ANN," *In Proc of 12th GAAS Symposium*, Amsrterdam pp. 427-430, 2004.

[14] M. S. Alam, and G.A.Armstrong, "An Analytical Approach for Extraction of Extrinsic HBT Parameter by Accurately Accounting the Distributed Nature of Base Resistance," Submitted in Year 2006 for publication in *Journal of Active and Passive Electronic Devices* (U.S.A.).

[15] Advance Design System (ADS), *Agilent Technologies*, 2003C,

[16] P. D. Tseng, L. Zhang, G. B. Gao, and M. F. Chang, "A 3-V Monolithic SiGe HBT Power Amplifier for Dual-Mode (CDMA/AMPS) Cellular Handset Applications", *IEEE Journal of Solid State Circuits*, vol. 35, no. 9, September pp. 1338-1344, 2000.

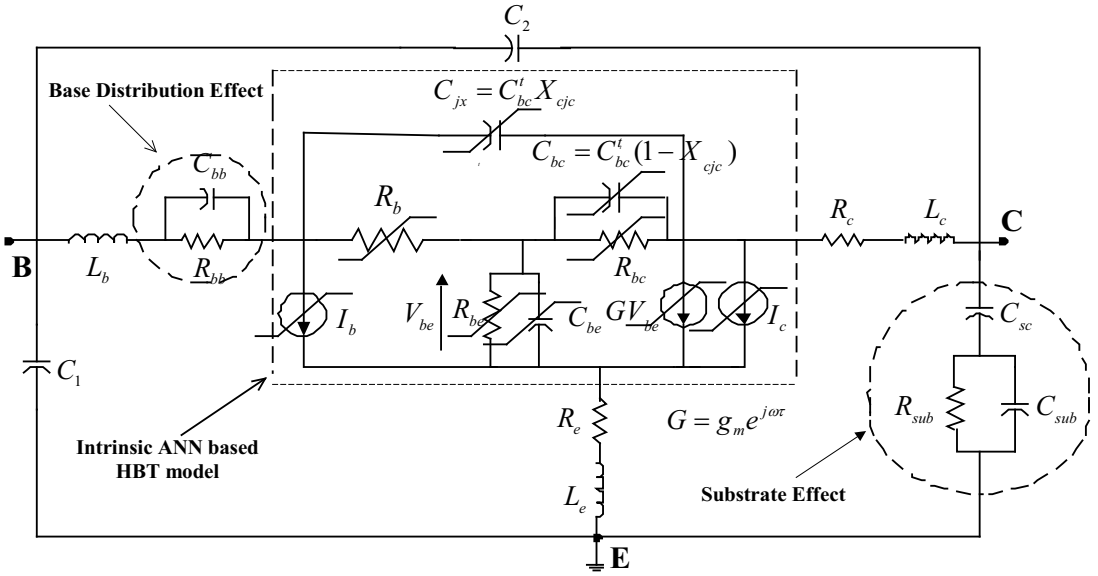

Fig. 1. Non-linear equivalent circuit model of HBTs

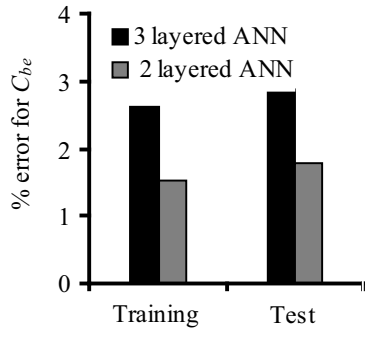

Fig. 2. Comparison of error performance of 03and 02 layered ANN architectures for C_{be}

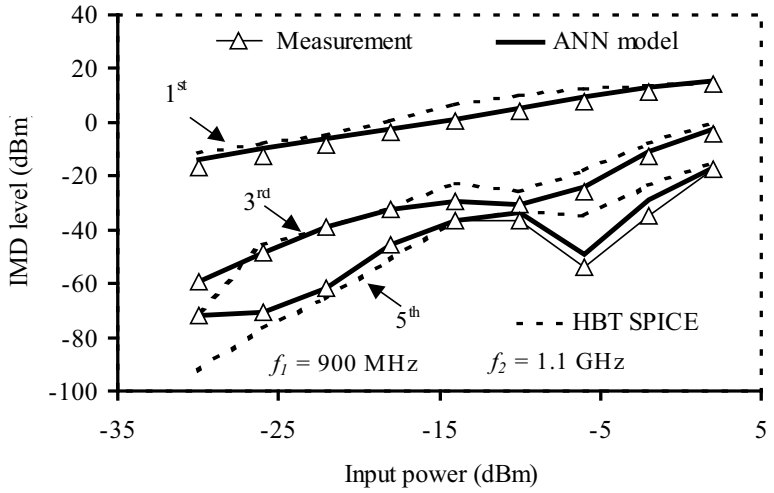

Fig. 3. Inter-modulation distortion (IMD) comparison of simulated and measured data (V_c = 3V and I_c = 5mA)

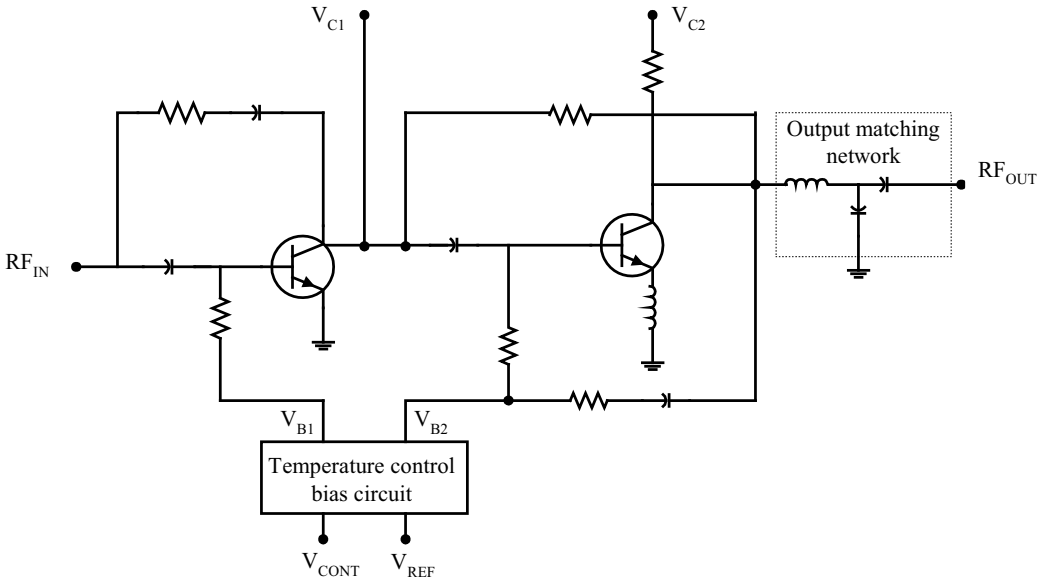

Fig. 4. Power amplifier circuit

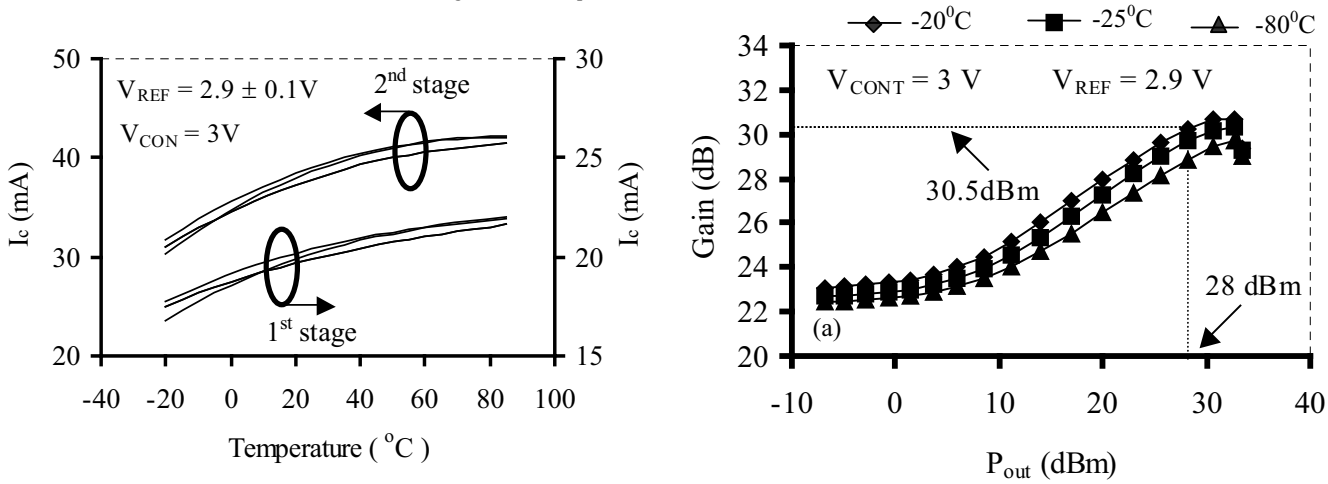

Fig. 5. Collector current I_c vs temperature in low mode of PA operation

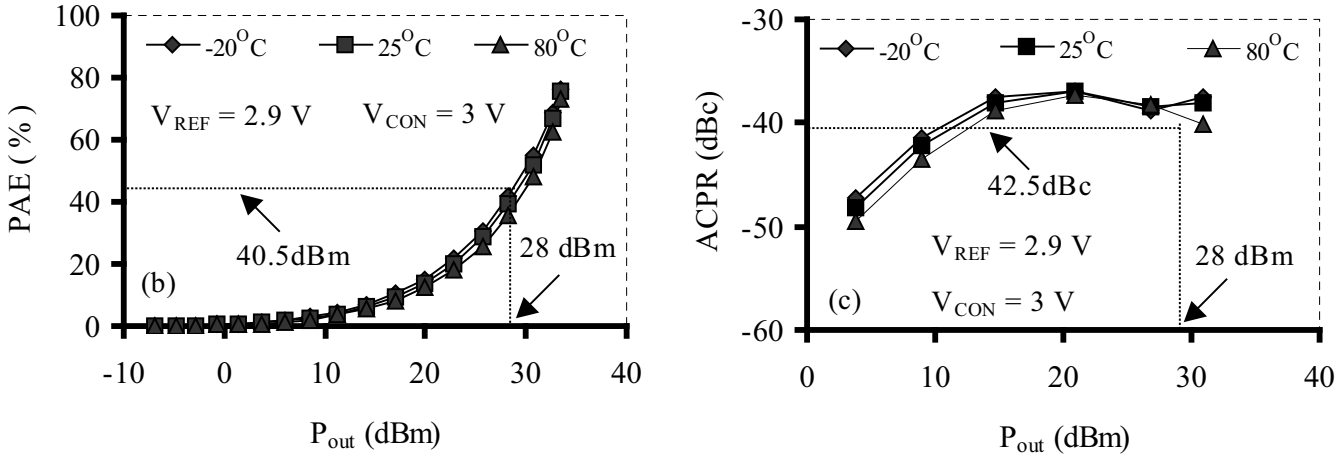

Fig. 6. PA module low mode performances for (a) power gain over temperatures and output power; (b) PAE over temperatures and output power c) ACPR over temperatures and output power