Exponentially Tapering Ground Wires for Elmore Delay Reduction in On Chip Interconnects

Mohammad Azim Karami
Nanoelectronics Center of Excellence
School of Electrical and Computer Engineering
University of Tehran
Tehran, Iran
Email: m.a.karami@ece.ut.ac.ir
Telephone:9821-2242-9583

Ali Afzali-Kusha
Nanoelectronics Center of Excellence
School of Electrical and Computer Engineering
University of Tehran
Tehran, Iran
Email: afzali@ut.ac.ir
Telephone:9821-8209-4359
Fax:9821-8877-8690

Abstract— **In this paper inter metal capacitors of ground wires are considered, for the first time in Elmore delay calculations of clock distribution interconnect networks. Analytical models for capacitance calculation of inter metal wires which are exponentially tapered are presented. In addition, the tapering of the ground wire for reducing this delay is proposed. The results show that by a exponentially tapering of the ground wires in the clock distribution networks , a 17% reduction in the Elmore delay of interconnects is achieved in compare with not tapering ground wires.**

***Index Terms*—Clock distribution network, Cross-talk, Elmore delay, Wire tapering**

I. Introduction

TECHNOLOGY scaling offers the benefits of reduced die area and improved transistor performance. The scaling however does not lead to reduction of the average wire length in circuits [1]. In addition, with interconnect scaling, the resistance and capacitance of interconnects increase leading to the rise of delay factors by about 40-60% per generation [1].

In general, the interconnect network consumes between 40 to 80 percent of the dynamic and static powers [2] while the clock distribution networks dissipates between 25 % to 70% [3] of power in today on chip systems.

One of the approaches to reduce the delay and power is the interconnect shaping (see, e.g., [4],[5]). H, Y, and X-tree clock distribution networks are widely used today for symmetric distribution of clock signals [6][7].

Exponentially H-tapered clock distribution networks has been introduced for reducing the Elmore delay and the power consumption [2][3][8][9]. Another phenomenon which affects the delay and power consumption of the clock network is its inductive impedance behavior as the signal frequency increases (the signal transition times decreases) [10]. A solution for decreasing the inductive behavior of the interconnects lines is shielding clock lines with adjacent ground lines [11][12]. This is shown in Fig 1.

One should note that with the technology scaling, the distance between interconnect lines decreases without much decrease in the interconnect thickness. This leads to the increase in inter metal capacitance in the same layer. This capacitance is becoming a dominant factor in forming the delay of interconnects in the state of the art digital systems [14].

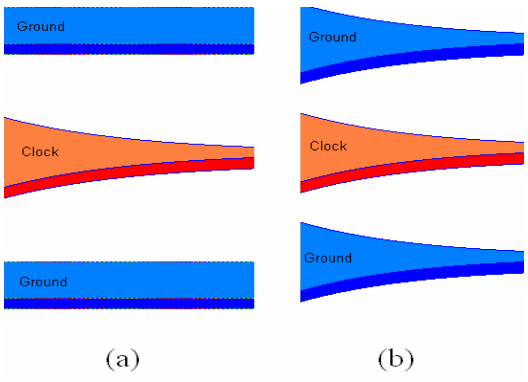


Fig. 1. (a) clock line tapering with flat ground wires (b) clock and ground wire tapering

In this paper, for the first time, we consider inter metal capacitors of ground wires in Elmore delay calculations of clock distribution interconnect networks.

Manuscript received May 29, 2006. This work was supported in part by University of Tehran.

M.A.Karami is with school of electrical & computer engineering of University of Tehran, Iran (corresponding author to provide phone:9821-2242-9583; e-mail: m.a.karami@ece.ut.ac.ir).

A.Afzali-Kusha is with school of electrical & computer engineering of University of Tehran, Iran (e-mail: afzali@ut.ac.ir).

1-4244-0765-6/06/$20.00 ©2006 IEEE

We also present analytical models for capacitance calculation of inter metal wires which are exponentially tapered.

We propose the use of exponentially tapered ground wires in the clock distribution networks for reducing the Elmore delay factor. This paper is organized as follows. In Section II, the Elmore delay model for the non-uniform wire thickness is briefly described. Section III contains the model for inter metal capacitance for different shapes of the clock and ground lines. The results of the Elmore delay when inter metal capacitance with different shapes are included are discussed in Section 4 while the summary and conclusion are given in Section 5.

II. Elmore Delay for Non-uniform Wire Width

Consider a wire segment *W* with the length of *L*, the width of *f(x)* at position *x*, a driver resistance of *Rd*, and the load capacitance of *CL*. This is depicted in Figure 2.

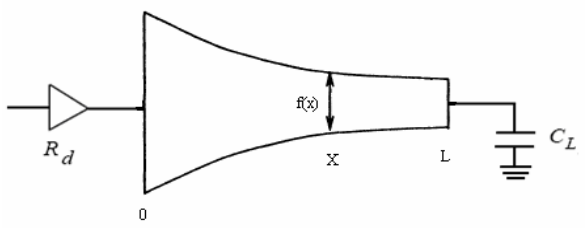


Fig. 2. Driver, load, and the interconnect line with variable width

The position dependent capacitance and resistance of the wire segments at position *x* are denoted by *C*(*x*) and *R*(*x*), respectively. The capacitance can be approximated by [16].

$$C(x) = (C_A + C_l(x_i) + C_f)\Delta x \quad (1)$$

Where C_f is the constant fringing capacitor between two layers or between an interconnect, and substrate (see Figure 3) $C_l(x_i)$ is the lateral capacitance (inter metal capacitance in interconnects) and C_A is the area capacitance. This capacitance is given by

$$C_A = c_0 f(x_i) \quad (2)$$

The model for inter metal capacitance will be presented in the next section for the exponentially tapered lines which are discussed in this paper. The fringing capacitance could be calculated using [15][16]

$$C_{fringing} = \varepsilon_{ox}[2.80(\frac{T}{H})^{0.222}] \quad (3)$$

Where ε_{ox} the dielectric constant of the insulator, T is is the thickness of wire and *H* is the distance from wire to bulk. The resistance is approximately given by

$$R(x) = r_0 \Delta x / f(x_i) \quad (4)$$

Where r_0 is the characteristic resistance of interconnect and Δx is the length of interconnect.

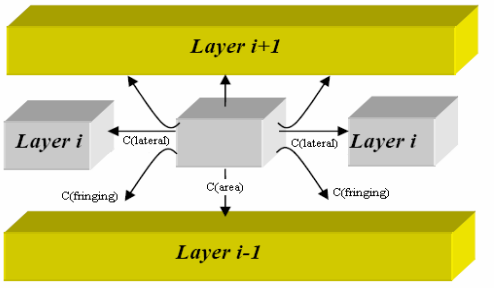


Fig. 3. Various components of the interconnect capacitance

The Elmore delay for the interconnect could be calculated using [8][19]

$$D_n = R_d(C_L + \sum_{i=1}^{n} c_0 f(x_i) + C_f + C_l(x)\Delta x)$$

$$+ \sum_{i=1}^{n} \frac{r_0 \Delta x}{f(x_i)} \left(\sum_{j=1}^{n} \left(c_0 f(x_j) + C_f + C_l(x_j) \right) \Delta x + C_L \right) \quad (5)$$

As $n \to \infty$ and $D_n \to D$, we can write

$$D = R_d(C_L + \int_0^L (c_0 f(x) + C_f + C_l(x))dx)$$

$$+ \int_0^L \frac{r_0}{f(x)} (\int_x^L ((c_0 f(t) + C_f + C_l(t))dt + C_L)dx \quad (6)$$

Using $f(x)$ in (6), one can calculate the Elmore delay for the interconnect wire.

III. Lateral (Inter Metal) Capacitance Model

In this section, the lateral capacitance between an exponentially tapered line and a flat line, and two exponentially tapered lines will be calculated. The exponentially tapered wire is in the form of

$$f(x) = we^{-ax} \quad (7)$$

Where *w* is the width of the line at *x* = 0 and *a* is the width decaying coefficient. To calculate this capacitance, we use the capacitance between two separate sheets shown in Fig 4. The capacitance is obtained from [17]

$$C_{lateral} = \frac{\varepsilon h}{\alpha} \ln(\frac{r_2}{r_1}) \quad (8)$$

Where α is the angle between the two sheets, *h* is the height of the sheet, and r_1 and r_2 define the length of the sheets.

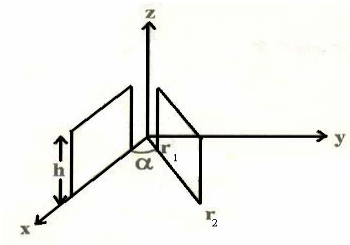


Fig. 4. Capacitance between two separate sheets

Using (8), we can express the differential capacitance due to a d*r* increase in the sheet length by

$$C_{lateral} = \frac{\varepsilon h}{\alpha}[\ln(\frac{r_2 + dr}{r_1}) - \ln(\frac{r_2}{r_1})] = \frac{\varepsilon h}{\alpha}\ln(\frac{r_2 + dr}{r_2}) \quad (9)$$

To use the above expression for the exponentially tapered interconnect layers, one should note that α is a function of position (r) and should be calculated. We denote the angle between a flat sheet and an exponential sheet by α_1 and between two exponential sheets α_2. The angles could be calculated using

$$\alpha_1 = \arctan(e^{-ar}) \quad (10)$$

$$\alpha_2 = 2 \times \arctan(e^{-ar}) \quad (11)$$

As $dr \to 0$, we can write (9) as

$$C_{lateral} = \frac{\varepsilon h}{\alpha}(1 + \frac{dr}{r}) \quad (12)$$

To derive (12), we have used the following approximation $\arctan(\alpha(r)) = \alpha(r)$ when $\alpha(r) \to 0$.

IV. Results and Discussion

To minimize the Elmore delay, the parameters of the exponentially tapered interconnect layer may be obtained by setting the derivative of (6) to zero after including the lateral capacitance obtained from (13). The derivative should be taken with respect to both w and a. (w is the width of the line at $x = 0$ and a is the width decaying coefficient, as mentioned in (7). The resulted equations lead to nonlinear equations which should be solved numerically. To perform the calculations for a practical clock distribution network, we consider $L = 300\mu m$, $r0 = 0.03\Omega/\mu m$, $c0 = 0.2\,fF/\mu m$, $C_f = 0.5\,fF/cm$, $R_d = 1\Omega$, $\varepsilon h = 9 \times 10^{-7} F$, and $C_L = 20\,fF$ [8].

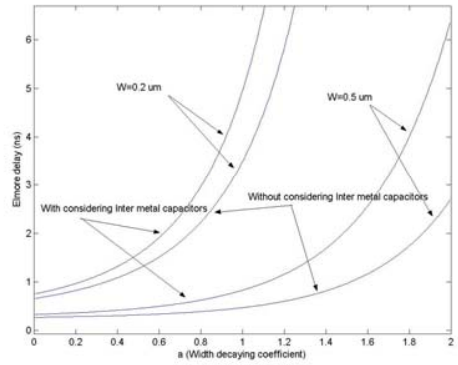
To study the effect of inter metal capacitance on the delay, the Elmore delay as a function these parameters has been plotted in Figure 5. As w and a increase the delay increases. As observed from the figure, neglecting the lateral capacitance causes non-negligible errors (under-estimation) in the delay calculation. Numerical methods should be used to find best w and a factors for delay minimization and finding the best factors of exponential tapering.

Figure 6 shows the efficiency of ground wire tapering scheme for Elmore delay reduction in interconnect distribution networks.

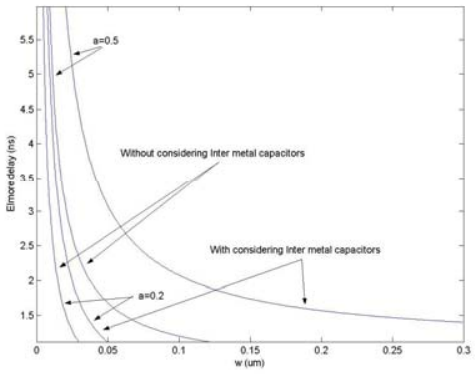
Figure 6 shows the Elmore delay with and without ground wire tapering scheme for Elmore delay reduction in the interconnect distribution networks. As inducted from this figure, the ground wire tapering will reduce the Elmore delay up to 17% when compared to a uniform ground wire width.

V. Summary and Conclusions

In this paper, we considered the effect of lateral (inter metal) capacitors in the Elmore delay of the interconnect distribution network for the first time. We presented an analytical expression for inter metal capacitance for exponentially tapered interconnect layer. We showed that neglecting the lateral capacitance led to an unacceptable error in the delay calculation. In addition, it was shown that exponentially tapering ground wires near clock distribution networks will result in a 17 percent reduction in the Elmore delay of the interconnect network with respect to uniform ground wire width.

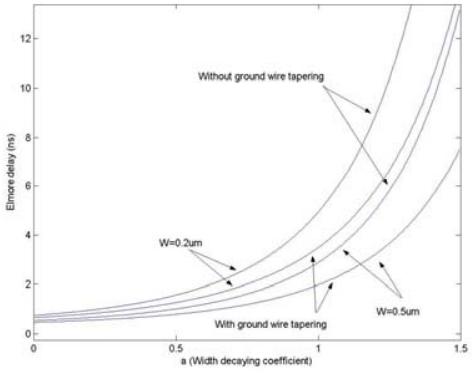


(a)

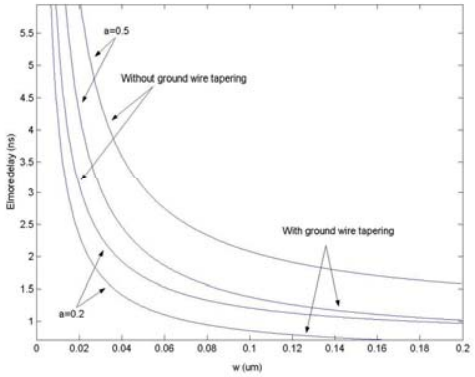


(b)

Fig. 5. The results for the Elmore delay with and without including the inter metal capacitance. The ground wire has a uniform width. (a) versus a, (b) versus w.



(a)



(b)

Fig. 6. Ground wire tapering efficiency in reducing the Elmore delay compared to a uniform ground wire. (a) versus *a*, (b) versus *w*.

REFERENCES

[1] W.Burleson "On chip interconnects: circuit and signaling from a MPSoC perspective," *Presentation at University of Massachusetts at Amhests* 2005

[2] Fei Li, Yan Lin and Lei He, "Vdd Programmability to Reduce FPGA Interconnect Power," *IEEE/ACM International Conference on Computer-Aided Design,* Nov. 2004

[3] M.A.El-Moursy and E.G. Freidman, "Exponentially Tapered H-Tree clock distribution networks,*" IEEE Transactions on VLSI,*pp.971-975 August 2005

[4] M.A.El-Moursy and E.G. Freidman, "Optimum wire shaping of an RLC interconnect," *Proc. IEEE Midwest Symp. on Circuits and Systems*, Dec. 2003.

[5] L. Vandenberghe, S. Boyd, and A. El-Gamal, "Optimal Wire and Transistor Sizing for Circuits with Non Tree Topology," In *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 252- 259, November 1997.

[6] H. Chen,C.k. Cheng, A. B. Kahng, I. I. Mandoiu, Q. Wang *and* B. Yao "The Y Architecture for On-Chip Interconnect Analysis and Methodology," *IEEE Trans on CAD of integrated circuits and systems* , vol. 24, no. 4, April 2005.

[7] S. Tam *et al.*, "Clock generation and distribution for the first IA-64 microprocessor," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1545–1552, Nov. 2000.

[8] J. P. Fishburn and C. A. Schevon, "Shaping a distributed-*RC* line to minimize Elmore delay," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 12, pp. 1020–1022, Dec. 1995.

[9] J. S. Roychowdhury, "Avoiding Dispersion in Distributed RLC Lines by Shaping," *Proceedings of the IEEE Multi- Chip Module Conference*, pp. I11-116, January 1995.

[10] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 7, no. 4, pp. 442–449, Dec. 1999.

[11] Y. Massoud *et al.*, "Managing on-chip inductive effects," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 6, pp. 789–798, Dec. 2002.

[12] P. J. Restle and A. Deutsch, "Designing the best clock distribution network," in *Proc. IEEE Int. Symp. on VLSI Circuits*, June 1998, pp. 2–5.

[13] Nagaraj NS "Interconnect modeling, signal integrity and reliability analysis for deep sub-micron integrated circuits," *PhD thesis, University of Texas at Dallas,* December 2003.

[14] J.C.T.Chen "Statistical modeling of MOSFETs and interconnects for Deep-submicron technologies," *PhD thesis , University of California, Berkeley*, Fall 1998.

[15] T. Sakurai and K. Tamaru, "Simple Formulas for Two- and Three-Dimensional Capacitances," *IEEE Trans. Electron. Device* ED-30,183-185, Feb. 1983.

[16] Chung-Ping Chen and D. F. Wong "Optimal Wire-Sizing Function with Fringing Capacitance Consideration," *Proc Design Automation Conference* pp. 604-607 1997.

[17] D. K. Cheng ,"Field and Wave Electromagnetics," Addison-Wesley series in electrical engineering, Winter 2002