A High Compliance Input and Output Regulated Body-Driven Current Mirror for Deep-Submicron CMOS

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***Abstract*—A current mirror circuit that uses body-driven MOSFETs to achieve an ultra-low input and output voltage is presented. High-gain amplifiers, suitable for a deep submicron process, are used to provide matching as well as input and output regulation. Simulation results were verified with measurements performed on a fabricated chip using the 90-nm CMOS process from ST-Microelectronics.**

***Index Terms*—Analog integrated circuits, CMOS, mirrors.**

I. Introduction

The current mirror (CM) remains a critical building block of analog VLSI circuits. In accordance with Moore's Law, MOSFET feature sizes continue to be reduced, which in turn increase the difficulties in designing high-performance analog circuits in deep-submicron technologies [1]. Supply voltage scaling reduces the amount of signal swing, with a lower limit being imposed by the threshold voltage, V_{TH} (which does not scale down at the same rate), further decreasing signal swing. In addition, channel-length modulation is increased as channel-length is reduced, leading to a low output resistance, r_o, and a low open-circuit gain [2]. Traditional cascode CM structures may improve r_o, but at the expense of signal swing, with $V_{out,min} = 2V_{DS,SAT}$. Low voltage (LV) operation is critically important, for example, when the CM is used as a built-in current sensor, e.g. IDDQ testing [3].

The use of body-driven (BD) techniques allows the minimum signal voltage imposed by V_{TH} to be circumvented [4]. In this paper, the BD technique is exploited to produce a high-compliance body-driven CM (BDCM) that employs input and output regulation for low and high output impedances, respectively. The BDCM architecture presented is suitable for use with deep-submicron (DSM) CMOS processes. A test chip was fabricated using the 90-nm process from ST-Microelectronics. The theoretical analysis, simulation results, and measured results are presented.

II. Body-Driven Current Mirror

A. Operating Principles

An ideal current mirror is characterized by low input impedance (R_{in}), high output impedance (R_{out}), and low voltage requirements on the input and output, i.e. high-compliance. Voltage regulation has been used to improve CM input [5] and output [6] impedances. High output-compliance regulated CMs can be achieved with various architectures [7].

A regulated BDCM topology removes the input voltage V_{TH} limitation while providing high output impedance [8]. However, input regulation can be used to further approach the ideal CM characteristics. The authors in [8] reduced the V_{DS} mismatch between a pair of triode-transistors, but the amplifier suggested did not provide a suitably high gain for a DSM process; this is addressed in the design described herein.

The proposed BDCM topology shown in fig. 1, uses BD MOSFETs M_1 and M_2 to provide the current mirroring. The typical gate-drain connected MOSFET seen in a CM is replaced by the body-drain connected one seen with M_1. For a given input current, I_{in}, V_{GS} of $M_{1,2}$ can be set high enough for triode operation. The required $V_{DS1,2}$ is thus low. The body terminal is slightly forward-biased and is only required to be at the low V_{DS} value to bias the CM. The V_{GS} of the BDMOSFETs is higher than V_{TH} yet is removed from the input path, whereas V_{DS} and V_{BS} remain in the input path but do not have any V_{TH} constraint. This is the key to the low input and output voltage capability.

For BD designs, the substrate typically has a forward-bias on the order of a few to tens of millivolts; conduction is in the pA range. $M_{1,2}$ were implemented in their own p-wells, via a deep n-well.

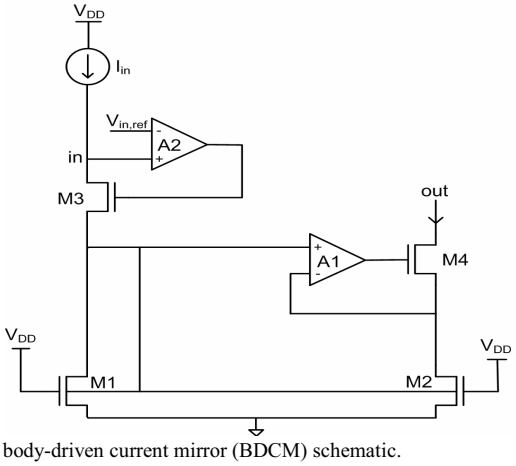

Fig. 1. A body-driven current mirror (BDCM) schematic.

The required V_{BS}, given by (4) for $M_{1,2}$ can be solved for using the triode-region I_{DS} equation and well-known body-effect equations, which are (1), (2), and (3) respectively. That is:

$$I_{DS} = \mu \cdot C_{ox} \frac{W}{L}(V_{GS} - V_{TH} - \frac{\alpha}{2}V_{DS})V_{DS} \quad (1)$$

$$\alpha = 1 + \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} \quad (2)$$

$$v_{TH} = v_{T0} + (\gamma\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad (3)$$

$$v_{BS} = \left[2\phi_F - 1/4\left(X + \sqrt{X^2 - v_{DS}}\right)^2\right] \quad (4)$$

$$X = -1/\gamma\left[i_{DS}/\left(\mu \cdot C_{ox}\frac{W}{L}v_{DS}\right) - v_{GS} + v_{T0} + v_{DS}/2 - \gamma\sqrt{2\phi_F}\right] \quad (5)$$

Amplifier A1 regulates the gate of M_4 to equalize $V_{DS1,2}$. This provides voltage matching, and thus better current mirroring. In addition, output impedance is increased, since V_{DS2} is held constant as V_{out} varies. Amplifier A2 regulates the gate of M*3* in order to set V_{in} equal to $V_{in,ref}$. Keeping V_{in} constant as I_{in} changes equates to a lowered input resistance.

For a given I_{DS}, as $V_{DS3,4}$ decreases, the required $V_{GS3,4}$ increases as given by (6), eventually causing the amplifiers to reach their saturation output voltage, V_{sat}; regulation is lost.

$$V_{sat} > V_{GS} = \frac{I_{DS}}{\mu C_{ox} W/L \cdot V_{DS}} + V_{TH} \quad (6)$$

The minimum output voltage is given as:

$$V_{out,\min} = V_{BS2} + V_{DS4,sat} \quad (7)$$

However, the output voltage can be decreased until A1 saturates. Referring to (6), if M_4 is sized such that V_{GS4} remains less than V_{sat} as V_{out} decreases, the amplifier doesn't saturate and a high R_{out} is maintained. In (12), a large A can compensate for a lower r_{o2}.

The minimum input voltage, $V_{in,min}$, is given by:

$$V_{in,\min} = V_{BS1} + V_{DS3,A2sat} \quad (8)$$

where $V_{DS3,A2sat}$ is the V_{DS3} that causes A2 to saturate. $V_{in,ref}$ is chosen such that $V_{DS3} < V_{DS3,A2sat}$. Note that in (8) a $V_{DS3,sat}$ is not required since a lower r_{o3} actually decreases R_{in}.

Using (1), the DC current transfer error, $\varepsilon = I_{out} - I_{in}$, is:

$$\varepsilon = \beta\left[(V_{GS1} - V_{TH})(V_{DS2} - V_{DS1}) + (V_{DS1}^2 - V_{DS2}^2)/2\right] \quad (9)$$

where $\beta = \mu C_{ox} W/L$ and C_{ox} is the capacitance of the oxide. It is assumed that $V_{GS1} = V_{GS2}$ and $V_{TH1} = V_{TH2} = V_{TH}$. Any difference in V_{DS} increases mismatch, and a reduction in V_{GS} reduces mismatch.

B. *Small-signal Analysis*

The small-signal analysis of the BDCM is straightforward. Without regulation, the input current delivered by a PMOS current source the small-signal current transfer ratio is:

$$\frac{i_{cs}}{i_{in}} = \frac{r_{op}}{r_{op} + (1/g_{mb}) \,||\, r_{on}} \quad (10)$$

where i_{cs} is the current source current and i_{in} is the current delivered to the mirror. Using realistic DC parameters for our process ($r_{op} = r_{on}$= 100kΩ and $1/g_{mb}$ = 30kΩ) the current transfer ratio is 0.81, but ideally it would be 1 if $R_{in} = 0$.

The output resistance, R_{out}, is given by:

$$R_{out} = g_{m4}r_{o2}r_{o4}(A+1) + g_{mb4}r_{o2}r_{o4} + r_{o2} + r_{o4} \quad (11)$$

$$R_{out} \approx g_{m4}r_{o2}r_{o4}A \text{ if A>>1} \quad (12)$$

where A is the amplifier gain.

The input resistance, R_{in}, is given by:

$$R_{in} = \frac{(1/g_{mb1} \,||\, r_{o1}) \cdot r_{o3}(g_{mb3} + g_{m3})}{g_{m3}r_{o3}A + 1} \quad (13)$$

Neglecting the body-effect of M_3, i.e. g_{mb3}, and assuming $(1/g_{mb1})||r_{o1} \approx 1/g_{mb1}$, and A >> $1/(g_{m3}r_{o3})$ we have:

$$R_{in} \approx \frac{1}{g_{mb1}A} \quad (14)$$

which improves the input resistance by a factor of A. Re-visiting (10) and assuming A=100k, the new R_{in} = 0.3 Ω which gives $i_{mirror}/i_{source} \approx 1$. Compared to [8], R_{in} is reduced by a factor of A. This is a vast reduction in the loading effect of the BDCM on previous stages.

C. *AmplifierDesign Criteria*

$M_{1,2}$ are in triode, and have a low r_o, therefore any difference in $V_{DS1,2}$ will cause a large and linear current mismatch. Therefore, a high-gain amplifier with minimal offset is critical for good mirroring. For DSM devices, this is a problem because they have a low open-circuit gain, $g_m r_o$; around 10 for the 90-nm devices used.

$V_{DS1,2}$ also operate near ground and so the input common-mode range (ICMR) must satisfy this requirement.

Lastly, the compliance can be maximized if the amplifiers have a maximized output voltage, V_{DD}.

The criteria above lead to the use of a gain-enhanced (GE), folded-cascode differential amplifier with a PMOS input stage and rail-to-rail output buffer. The GE amplifiers use a cascode structure to further improve the gain. However, due to their limited gain, a systematic offset is introduced. The amplifiers designed had a gain of 110 dB, phase margin of 108 degrees, f_{unity} of 86 MHz, and a systematic offset of 127 µV.

III. Simulation Results

Simulation was performed using Spectre and the 90-nm device models provided in the CMOS-90 design-kit. To further decrease the required input and output voltages for a given I_{DS}, the MOSFET sizes were made relatively large. There is a trade-off between area and compliance. For PMOS, the ratio, in microns, was 26.88/0.2, and for NMOS, 11.52/0.2. The minimum W and L are 0.12 and 0.1 µm, respectively. The supply voltage, V_{DD}, is 1 V. A p-well/n-well diode representing the BDMOSFET well junction capacitance was included.

The plot of I_{out} vs. V_{out} is shown in Fig. 2. Current source behavior begins at an ultra-low voltage of 1.4 mV. The output resistance, R_{out}, rapidly enters the MΩ range and reaches 360 MΩ, as shown in fig. 3.

Fig. 2 shows also a comparison between the proposed BDCM, a prior regulated output BDCM [8], and a simple CM all designed with 90-nm devices. The performance of [8] in a 90-nm process is severely degraded due to the very low-gain amplifier used, with an approximate gain of A = $g_m r_o/2$. R_{out} is improved by over 3 orders of magnitude.

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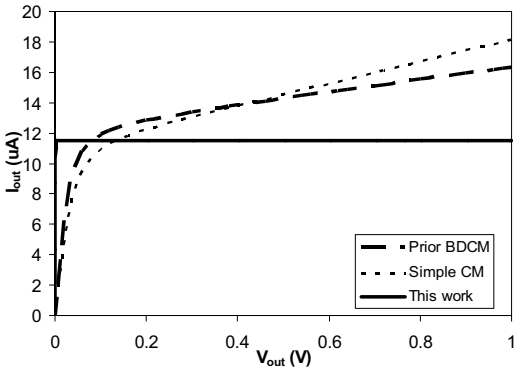

Fig. 2. I_{out} vs. V_{out} – Comparison of current mirrors.

The DC current transfer curve, shown in fig. 4, indicates that there is an 8.8 µA offset in current. There is a high degree of linearity (i.e. a variation in I_{in} causes an equal change in I_{out}); the average slope of fig. 4 is 1.0012. The drain voltages of the BDMOSFETs, M_1 and M_2 are 1.16 mV and 660.5 µV, respectively. For $M_{1,2}$, the sensitivity to $V_{DS1,2}$ is 17 µA/mV.

Fig. 5 shows R_{in} vs. I_{in}. An ultra-low R_{in} of approximately 20 mΩ is maintained until the amplifier saturates, at which point, R_{in} approaches 120 Ω. The saturation point can be increased by increasing $V_{in,ref}$. For simulations purposes $V_{in,ref}$ is set to 20 mV.

The frequency response, shown in fig. 6, indicates that the 3dB roll-off is 83 kHz. The AC reference current has a value of 1, which sets the input branch current, which is then mirrored by the output branch. There is a small current gain due to the channel-length modulation between the bias reference and input branch currents; the current is not applied directly.

IV. FABRICATION RESULTS

The BDCM was fabricated with the ST-Microelectronics CMOS090 platform. This is a 7-metal, single-poly process. The area of the die is 0.7151 X 0.7266 mm^2. Testing was carried out on the packaged (24-pin DIP) parts. A 24 kΩ external resistor is used to set all internal bias voltages and currents. The total power consumption is 2.3 mW. Core and I/O circuitry have separate supplies. Current mirror and differential-amplifier transistor pairs were split and laid out in a common centroid configuration to reduce mismatch due to doping and thermal gradients. For multi-fingered devices, dummy poly strips are used.

The input and output current is shown in Fig. 7. The compliance is 40 mV and a reverse current of 4.3 µA occurs at V_{out} = 0 V. With a non-zero ground voltage for M_2, a reverse current flows. The non-zero voltage is caused by *IR* drop on the ground line.

Current mismatch was mitigated by using $V_{GS1,2}$ = 0.32 V. There is a trade-off between compliance and the mirroring offset. The reduced $V_{GS1,2}$ increases R_{out}, since the devices are not as heavily in the triode region. The average R_{out} is 10 GΩ.

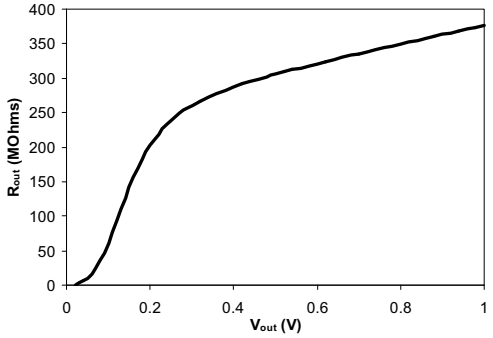

Fig. 3. R_{out} vs. V_{out} – output resistance characteristic.

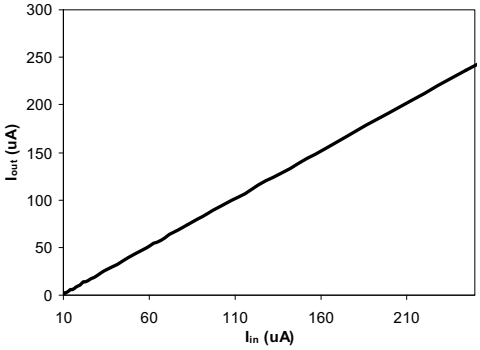

Fig. 4. I_{out} vs. I_{in} – DC current transfer characteristic.

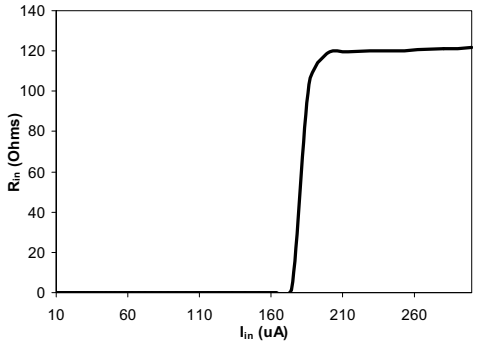

Fig. 5. R_{in} vs. I_{in} - Input resistance characteristic.

The peak-to-peak current fluctuation is 1.4 uA and the RMS value is 0.23 uA. This is a deviation from the mean value (22.7 uA) of 1.01%.

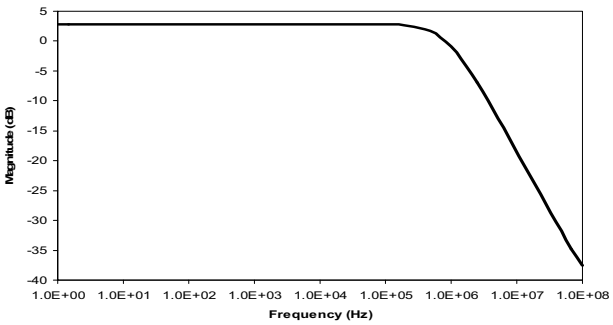

Fig. 6. I_{out}/I_{ref} vs. frequency – AC response.

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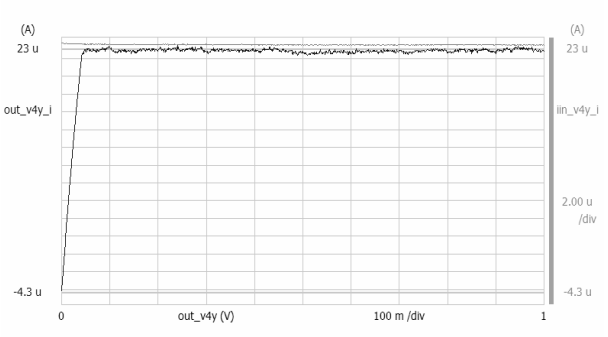

Fig. 7. I_{out}, I_{in} vs. V_{out} – Output current characteristic.

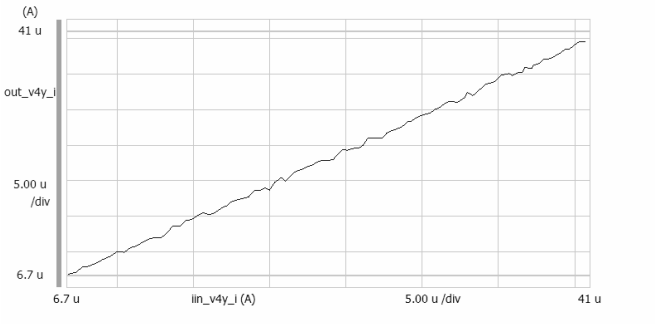

Fig. 8. I_{out} vs. I_{in} – DC current transfer characteristic.

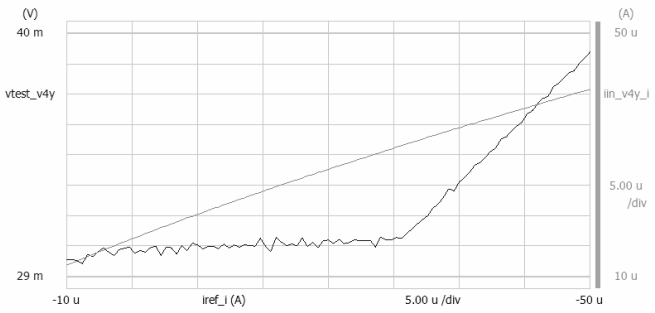

Fig. 9. V_{in}, I_{in} vs. I_{ref} – Input voltage regulation.

The current transfer curve is shown in Fig. 5. The slope of curve is 1.02. The average value of $I_{out} - I_{in}$ is 0.7 µA .The bias current I_{ref} is used to modulate I_{in}, as shown in Fig. 6, and the resulting average input resistance is 0.5 mΩ.

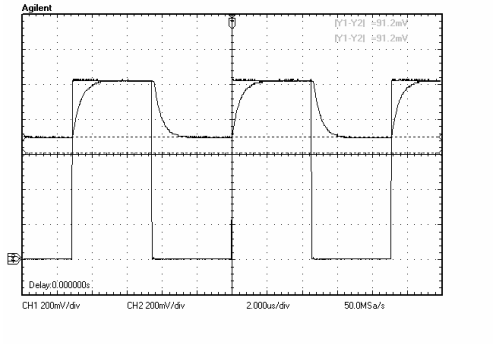

Fig. 10. Large-signal stability test.

Large-signal stability is tested by applying a 110 kHz, 1 V square wave, as shown in fig. 10. The output load is 17 kΩ. The same load was used to yield a frequency response with a 3dB rolloff of 300 kHz. Finally, a photograph of the fabricated packaged chip is shown in fig. 11 along with the bonding wires.

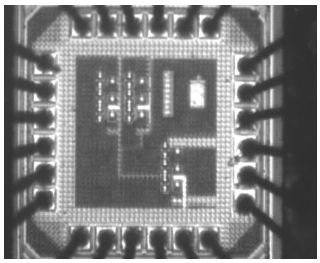

Fig.11. Photo of 90-nm CMOS BDCM test chip.

V. Conclusion

The regulated input, regulated output CM topology implemented with high-gain amplifiers offers low input and high output impedance. Also, the input and output voltage requirements are lowered via body-driven MOSFETs.

Acknowledgments

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Top