ICS 233 – Computer Architecture & Assembly Term 101 – Fall 2010

Pipelined Processor Project Evaluation Form

	Student Name / ID	Grade	Remarks	Bonus/Penalty
ers				
Members				
Σ				

	Section	Grade	Max	Remarks
0 pts)	ALU Implementation		10	
	Register File Implementation		5	
ntrol (5	Datapath and Control		10	
Components and Control (50 pts)	Correct implementation of individual ALU instructions (R-type and I-type)		10	Instructions are tested separately
ponents	Correct implementation of LW and SW instructions.		5	
Com	Correct implementation of BEQ, BNE, and J instructions		5	
	Correct implementation of JAL and JR instructions		5	
0 pts)	Instructions are pipelined properly with their control signals		10	
Pipelining (30 pts)	Forwarding implemented properly		10	
Pipe]	Stalling pipeline (load delay, branch)		10	
	Writing Style, Spelling, Grammar		5	
(20 pts)	Design Description & Drawings		5	
Report	Test cases, verifying correct execution		5	
	Describing group work, meetings, and contributions of the group members		5	