ICS 233 - Computer Architecture & Assembly Language

Exam II – Fall 2007

Saturday, December 8, 2007
7:00 pm – 9:00 pm

Computer Engineering Department
College of Computer Sciences & Engineering
King Fahd University of Petroleum & Minerals

Student Name: _____

Student ID: _____

Q1	/ 15	Q2	/ 15
Q3	/ 25	Q4	/ 20
Q5	/ 25		
Total	/ 100		

Important Reminder on Academic Honesty

Using unauthorized information or notes on an exam, peeking at others work, or altering graded exams to claim more credit are severe violations of academic honesty. Detected cases will receive a failing grade in the course.

Q1. (10 pts) Using the refined multiplication hardware, show the **unsigned** multiplication of:

Multiplicand = **`01101101`** by Multiplier = **`10110110`**

The result of the multiplication should be a 16 bit unsigned number in HI and LO registers. Eight iterations are required. Show your steps.

b) (5 pts) What is the decimal value of the following floating-point number?

`1 10001101 10101000000000000000000` (binary)

Q2. (10 pts) Using the refined division hardware, show the **unsigned** division of:

Dividend = **`11011001`** by Divisor = **`00001010`**

The result of the division should be stored in the Remainder and Quotient registers. Eight iterations are required. Show your steps.

b) (5 pts) Show the **Double precision** IEEE 754 representation for: **`-0.05`**

Q3. Given $x = \mathtt{1\ 10000101\ 10110000000000000000001}_2$
and $y = \mathtt{1\ 01111111\ 01000000000000011000000}_2$
represent single precision floating-point numbers. Perform the following operations showing all the intermediate steps and final result in binary. Round to the nearest even.

a) (12 pts) $x + y$

Q3. b) (13 pts) $x \times y$

Q4. (20 pts) A program, being executed on a processor, has the following instructions mix:

Operation	Frequency	Clock cycles per instruction
ALU	40 %	2
Load	20 %	10
Store	15 %	4
Branches	25 %	3

a) (3 pts) Compute the average clock cycles per instruction

b) (6 pts) Compute the percent of execution time spent by each class of instructions

c) (6 pts) A designer wants to improve the performance. He designs a new execution unit that makes 80% of ALU operations take only **1** cycle to execute. The other 20% of ALU operations will still take **2** cycles to execute. The designer also wants to improve the execution of the memory access instructions. He does it in a way that **95%** of the **load** instructions take only **2** cycles to execute, while the remaining **5%** of the **load** instructions take **10** cycles to execute per **load**. He also improves the store instructions in such a way that each **store** instruction takes **2** cycles to execute.

Compute the new average cycles per instruction

d) (2 pts) What is the speedup factor by which the performance has improved in part **c**?

e) (3 pts) The designer decides to improve the clock speed in such a way to **triple** the overall performance of the original CPU specified in part **a**.

By what factor should the clock rate be improved if the designer uses the design specified in part **c**?

Q5. (25 pts) The following code fragment processes two double-precision floating-point arrays *A* and *B*, and produces an important result in register **`$f0`**. Each array consists of **`10000`** double words. The base addresses of the arrays *A* and *B* are stored in **`$a0`** and **`$a1`** respectively.

```
        ori     $t0, $zero, 10000
        sub.d   $f0, $f0, $f0

loop:   ldc1    $f2, 0($a0)
        ldc1    $f4, 0($a1)
        mul.d   $f6, $f2, $f4
        add.d   $f0, $f0, $f6
        addi    $a0, $a0, 8
        addi    $a1, $a1, 8
        addi    $t0, $t0, -1
        bne     $t0, $zero, loop
```

a) (6 pts) Write the code in a high-level language, and describe what is produced in **`$f0`**.

c) (5 pts) Count the total number of instructions executed by all the iterations (including those executed outside the loop).

d) (14 pts) Assume that the code is run on a machine with a **2 GHz** clock that requires the following number of cycles for each instruction:

Instruction	Cycles
`addi, ori`	1
`ldc1`	3
`add.d, sub.d`	5
`mul.d`	6
`bne`	2

(7 pts) How many cycles does it take to execute the above code?

(3 pts) How many second to execute the above code?

(2 pts) What is the average CPI for the above code?

(2 pts) What is the MIPS rate for the above code?