COE 502/CSE 661 Syllabus – Fall 2007
Parallel Processing Architectures

Computer Engineering Department
College of Computer Sciences & Engineering
King Fahd University of Petroleum & Minerals

Professor: Muhamed Mudawar, Room 22/328, Phone 4642
Office Hours: SMW 10 am – 12 noon or by appointment
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Catalog Description

Introduction to parallel processing architectures, sequential, parallel, pipelined, and dataflow architectures. Vectorization methods, optimization, and performance. Interconnection networks, routing, complexity, and performance. Small-scale, medium-scale, and large-scale multiprocessors. Data-parallel paradigm and techniques. Multithreaded architectures and programming. The students are expected to carry out research projects in related field of studies.

Prerequisites: COE 308 or equivalent.

References

John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, Fourth Edition, Morgan Kaufmann Publishers, 2006, ISBN: 0-12-370490-1

David E. Culler, Jaswinder Pal Singh, with Anoop Gupta, *Parallel Computer Architecture: A Hardware/Software Approach*, Morgan Kaufmann Publishers, 1999, ISBN: 1-55860-343-3.

Course Description

This course provides an in-depth study of the design, engineering, and evaluation of modern parallel computers. It begins with an overview of the field focusing on the convergence of many diverse architectural approaches. It extracts fundamental design issues: naming, replication, synchronization, latency, overhead, and bandwidth and explores these across the spectrum of modern machines. It studies small-scale shared memory multiprocessors in some detail. It then examines scalable multiprocessors thoroughly, including realizing programming models via network transactions, directory-based cache coherence, and interconnection network design. There will be a term project resulting in a research paper.

Course Topics

Introduction to Parallel Architectures

Why Parallel Architectures
Diversity and Convergence of Parallel Architectures
Fundamental Design Issues

Parallel Programming and Workload-Driven Evaluation

The Parallelization Process
Workload-Driven Evaluation

Cache Coherent Bus-Based Multiprocessors

Cache Coherence and Bus Snooping
Design Space for Snooping Protocols
Single-Level Caches with an Atomic Bus
Multilevel Cache Hierarchies
Split-Transaction Bus Design

Memory Consistency

Sequential Consistency
Relaxed memory consistency models

Synchronization

Mutual Exclusion, Event, and Barrier Synchronization
Algorithms for locks and barriers

Directory-Based Cache Coherent Multiprocessors

Directory-Based Approaches
Memory-Based Directory Protocols
Cache-Based Directory Protocols
Hierarchical Coherence

Vector Processors

Vector Programming Model
Vector Instruction Set and its advantages
Vector Arithmetic Execution
Vector Memory System

Interconnection Networks

Organizational Structure
Topologies
Routing
Switch Design
Flow Control
Communication Performance

Paper Assignment

Selected papers will be assigned throughout the semester. A two-page summary should be submitted for each assigned paper. The main points and contributions should be identified and discussed. Students will take turn presenting papers. Each presentation will not exceed 20 min.

Research Project

A research project will be conducted during the semester in groups of two or three students. A subject should be first selected and surveyed. Papers should be reviewed about the selected subject. A simulation should be conducted and performance results should be obtained. Your work should be reported in the form of a research paper. A 20-minute presentation will be given to each group during the last week of the semester.

Grading Policy

Assignments and Presentations:	10%
Research Project:	40%
Midterm Exam:	25%
Final Exam:	25%