COE 308 – Computer Architecture, Fall 2011

Pipelined Processor Project Evaluation Form

	Student Name / ID	Grade	Remarks	Bonus/Penalty
Members				

	Section	Grade	Max	Remarks
Components and Control (40 pts)	ALU Implementation		5	
	Datapath and Control		10	
	Correct implementation of all ALU instructions (R-type and I-type)		10	**Instructions are tested separately**
	Correct implementation of LW and SW instructions.		5	
	Correct implementation of BEQ, BNE, and J instructions		5	
	Correct implementation of JAL and JR instructions		5	
Pipelining (35 pts)	Instructions are pipelined properly with their control signals		15	
	Forwarding implemented properly		10	
	Stalling pipeline (load delay, branch)		10	
Poster & Report (25 pts)	Poster Quality		10	
	Report Quality		10	
	Demo, providing sufficient test cases		5	