

COE 308 – Computer Architecture

Syllabus for Fall 2011

Computer Engineering Department
College of Computer Sciences & Engineering
King Fahd University of Petroleum & Minerals

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Catalog Description

Memory hierarchy and cache memory. Integer and floating point arithmetic. Instruction and arithmetic pipelining, superscalar architecture. Reduced Instruction Set Computers. Parallel architectures and interconnection networks.

Prerequisites: COE 205.

Textbook

David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware / Software Interface*, Fourth Edition, Morgan Kaufmann Publishers, 2009.

Course Objectives

- In-depth understanding of the inner-workings of modern computer systems, their evolution, and tradeoffs present at the hardware-software interface.
- Understanding the design process of a modern computer system. This includes the design of the processor datapath and control, the memory system, and I/O subsystem.

Grading Policy

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| Quizzes | 10% |
| MIPS Programming | 15% |
| CPU Design Project | 20% |
| Major I Exam | 15% |
| Major II Exam | 20% |
| Final Exam | 20% |

Software Tools used in Mini-Projects

- MARS simulator: runs MIPS-32 assembly language programs.
- LogiSim simulator: educational tool for designing and simulating CPUs.

Course Topics and Lecture Breakdown by Week

| Week | Course Topics |
|-------|---|
| 1 | Introduction to computer architecture, ISA versus organization, components, abstraction, technology improvements, chip manufacturing process. |
| 2-4 | Instruction set design, RISC design principles, MIPS registers, instruction formats, arithmetic instructions, immediate operands, bit manipulation, load and store instructions, byte ordering, addressing modes, flow control instructions, pseudo-instructions, procedures and runtime stack, call and return, MIPS register conventions, alternative architecture, ARM, Intel. |
| 5 | CPU performance and metrics, CPI, performance equation, MIPS as a metric, Amdahl's law, benchmarks and performance of recent Intel processors. |
| 6-7 | Integer multiplication, integer division, floating point representation, IEEE 754 standard, normalized and de-normalized numbers, zero, infinity, NaN, FP comparison, FP addition, FP multiplication, rounding and accurate arithmetic, FP instructions in MIPS. |
| 8-9 | Designing a processor, register transfer logic, datapath components, clocking methodology, single-cycle datapath, main control signals, ALU control, single-cycle delay, multi-cycle instruction execution, Multi-cycle versus single-cycle execution. |
| 10 | Pipelining versus serial execution, MIPS 5-stage pipeline, pipelined datapath, pipelined control, pipeline performance. |
| 11 | Pipeline hazards, structural hazards, data hazards, stalling pipeline, forwarding, load delay, compiler scheduling, hazard detection, stall and forwarding unit, control hazards, branch delay, dynamic branch prediction, branch target and prediction buffer. |
| 12-13 | Cache memory design, locality of reference, memory hierarchy, DRAM and SRAM, direct-mapped, fully-associative, and set-associative caches, handling cache miss, write policy, write buffer, replacement policy, cache performance, CPI with memory stall cycles, AMAT, two-level caches and their performance, main memory organization and performance. |
| 14 | Introduction to Parallel Architectures |