COE 308 – Computer Architecture

Term 091 – Fall 2009

Pipelined Processor Project Evaluation Form

	Student Name / ID	Grade	Remarks	Bonus/Penalty
Members				

	Section	Grade	Max	Remarks
Components and Control (50 pts)	ALU Implementation		**10**	
	Register File Implementation		**5**	
	Datapath and Control		**10**	
	Correct implementation of individual ALU instructions (R-type and I-type)		**10**	**Instructions are tested separately**
	Correct implementation of LW and SW instructions.		**5**	
	Correct implementation of BEQ, BNE, and J instructions		**5**	
	Correct implementation of JAL and JR instructions		**5**	
Pipelining (30 pts)	Instructions are pipelined properly with their control signals		**10**	
	Forwarding implemented properly		**10**	
	Stalling pipeline (load delay, branch)		**10**	
Report (20 pts)	Writing Style, Spelling, Grammar		**5**	
	Design Description & Drawings		**5**	
	Test cases, verifying correct execution		**5**	
	Describing group work, meetings, and contributions of the group members		**5**	