Characteristics of Logic Gates

COE 202
Digital Logic Design
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Presentation Outline

- Timing Diagrams
- Gate Delay and Circuit Delay
- Fan-In and Fan-Out
Voltage Levels

- Logic 1 is a range of voltage values
  - NOT just a single voltage value
- Logic 0 is also a range of voltages
  - Not just zero volt
- The voltage range between logic 0 and 1 is undefined
- Digital signals are not allowed to use voltage values in the undefined range
Timing Diagram

- Shows the logic values of signals in a circuit versus time
- **Waveform**: the shape of a signal over a period of time
- Example: timing diagram of an AND gate (with zero delay)

![Timing Diagram of an AND gate with zero delay](image)
A change in the inputs of a gate causes a change in its outputs. However, the change in the output signal is **not instantaneous**. There is a small delay between an input signal change and an output signal change, called **gate delay**.

![Gate Delay Diagram]

Gate delay = $\tau$

Where $x$, $y$, and $z$ are the input and output signals, and $\tau$ represents the delay time.
In a given circuit, each gate has a delay

The circuit has a propagation delay between inputs and outputs

The propagation delay is computed along the critical path

To compute the propagation delay, start at the inputs:

1. Delay at each gate output = Maximum input delay + Gate delay
2. Propagation delay of a circuit = maximum delay at any output
Computing the Maximum Circuit Delay

- Consider the following circuit with 8 inputs and 2 outputs
- Delay of a 2-input AND gate = 2 ns
- Delay of a 3-input AND gate = 3 ns
- Delay of a 2-input OR gate = 2 ns
- Delay of a 3-input OR gate = 3 ns

Compute the Maximum Circuit Delay
Rise-Time and Fall-Time

- In logic simulators, a waveform is drawn as an **ideal wave**
- The change from 0 to 1 (or from 1 to 0) is instantaneous
- In reality, a signal has a non-zero **rise-time** and **fall-time**
  - Time taken to change from 10% to 90% of High voltage (and vice versa)
Fan-In

- The **fan-in** is the number of inputs to a gate
- Example: a 3-input AND gate has a Fan-in of 3
- Logic gates with a large fan-in tend to be slow
- Increasing the Fan-in of a gate increases the gate delay
- For example, a 3-input AND gate has a higher delay than a 2-input AND gate made with the same technology
- Using logic gates with higher fan-in is useful when reducing the depth (number of levels) of a logic circuit
Fan-Out

- In digital circuits, it is common for the output of one gate (called **driver gate**) to be connected to the inputs of several **load gates**.

- The **fan-out** of a gate is the number of gate inputs it can feed.

- There is a limit on the maximum fan-out of a gate.

The output of a driver gate can supply a limited amount of current.

Each input of a load gate consumes a certain amount of current.

Therefore, the driver gate can only feed a limited number of load gates.

**Fan-Out = 2**

![Diagram](image.png)
Increasing the Fan-Out with a Buffer Gate

- **Buffer Gate**
  - Output $f = \text{Input } x$

- **Buffer provides drive capability**
  - Used to amplify an input signal
  - High current output
  - Increases the Fan-Out

- **Buffer gate increases the propagation delay of a circuit**