King Fahd University of Petroleum and Minerals

College of Computer Science and Engineering

Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 171 (Fall 2017)
Final Exam
Monday, January 8th, 2018

Time: 120 minutes, Total Pages: 10

Name:________________________________ ID:____________________ Section: _______

Notes:
Do not open the exam book until instructed
Calculators are not allowed (*basic, advanced, cell phones, etc.*)
Answer all questions
All steps must be shown
Any assumptions made must be clearly stated

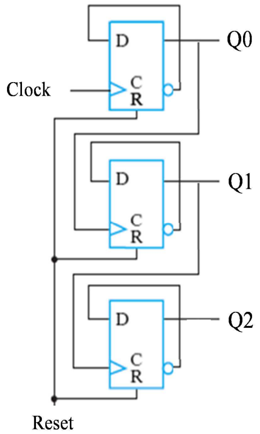
Question	Maximum Points	Your Points
1	25	
2	10	
3	15	
4	12	
5	8	
6	10	
7	15	
Total	95	

Question 1: **[25 points]**

a) For a basic NOR SR latch the input SR = ________ keeps the state of the latch unchanged, while the forbidden input is SR = _______ **(2 points).**

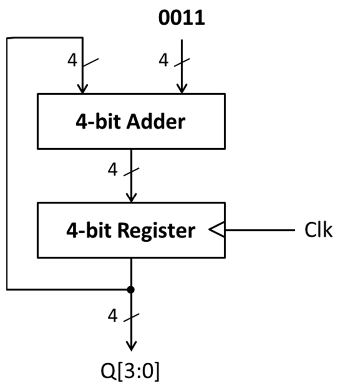
b) The shown 3-bit binary counter counts **upwards/downward** (circle one).

The counter has a maximum count of _________and a minimum count of ___________ **(3 points)**.



c) Given the following block diagram below:

If the output Q is 1 during the current cycle *t*, shown the output Q at (*t*+1) after 1 cycle, and at (*t*+2) after 2 cycles. **(2 points)**

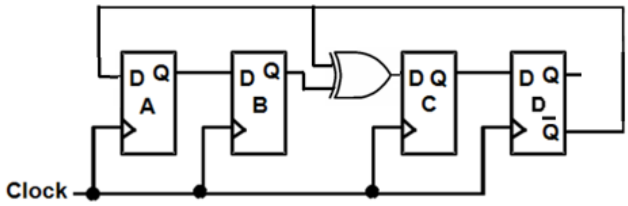


Q(*t*)	Q(*t*+1)	Q(*t*+2)
0001		

Describe the function of the circuit in the above diagram: **(1 points)**

d) The 4-bit shift register shown was initially loaded with ABCD = 0100. List in the table below the contents of the register after receiving each of the clock pulses indicated. **(2 points).**

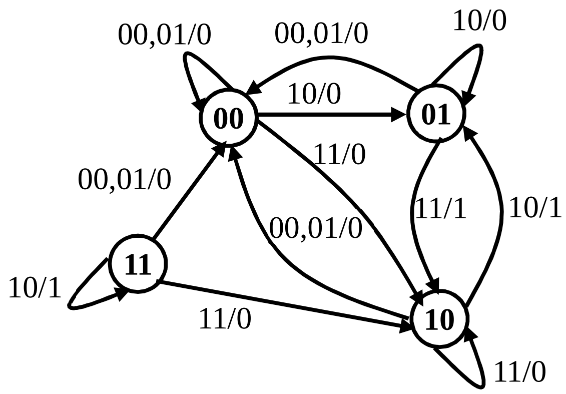
	Register Contents A B C D (Binary)
Initial	0 1 0 0
After Clock Pulse 1	
After Clock Pulse 2	



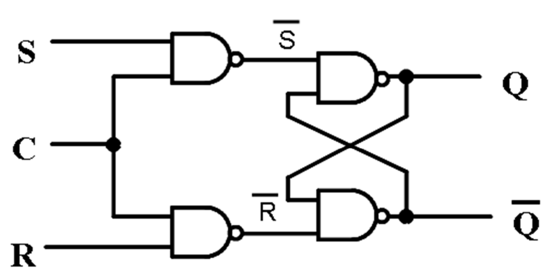
e) A sequential circuit has two inputs; ***X*** and ***Y,*** and one output ***Z*** and the state diagram below:

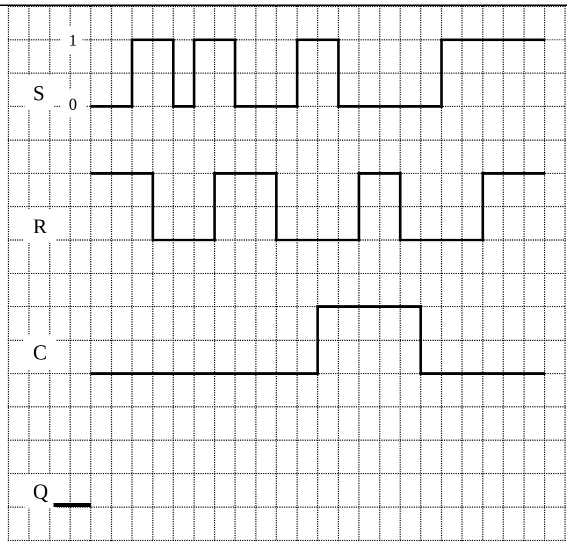
- The ***synchronous reset*** input is ________ (***X or Y***?) The circuit is reset when this input is ***High/Low*** (circle one) and the ***reset state*** is ____________ The **unused state** is ____________ **(4 points)**

- For the input sequence **00 then 11 then 11 then 10,** the circuit would **end up in state** __________ **(1 point)**

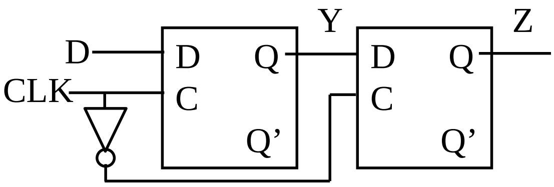


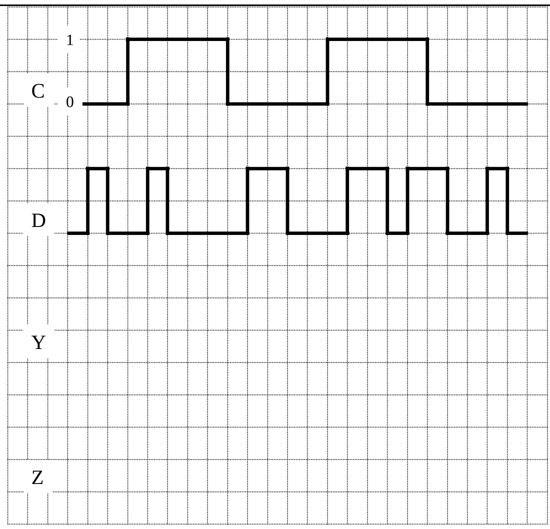
f) For the clocked SR latch shown, complete the waveform of the Q output for the given S, R, and clock (C) inputs. Initially, Q is 0. Ignore any propagation delays. **(2 points).**





g) Given the master-slave D-FF shown in Figure, complete the timing diagram for signals Y and Z (assume they are both initially at 0 and ignore any propagation delays. **(4 points).**





h) Given a synchronous sequential circuit with 13 states, the minimum number of flip flops required to implement the circuit is __________ flip flops and the number of unused states is __________ states.

(2 points)

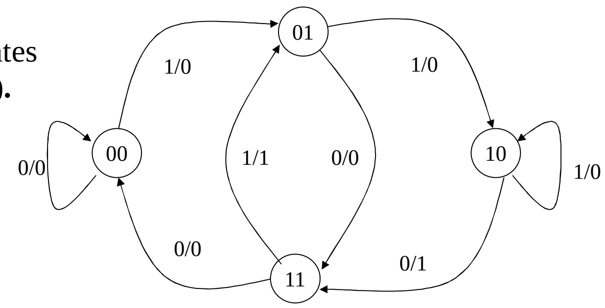
i) For a 5-bit synchronous binary counter with outputs Q4, Q3, Q2, Q1, and Q0 (where Q0 is the least-significant bit), if the clock frequency is **800** MHz then the frequency of Q2 is ___________ MHz and the frequency of Q4 is ___________ MHz. **(2 points)**

Question 2. **[10 points]**

Draw the state diagram of a **<u>Moore</u>** synchronous sequential circuit that receives a serial input **y** and produces a serial output **z**. The output *z* should be **1** when the circuit detects the sequence **01100**. Overlapping sequences **are allowed**. A sample input/output trace after a reset is shown below:

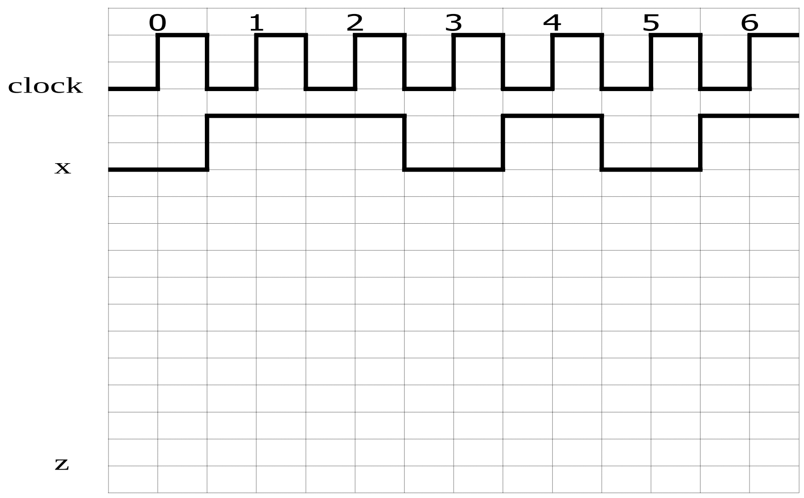
y	0	1	1	0	0	1	1	0	0	0	1	
z	0	0	0	0	0	1	0	0	0	1	0	0

Question 3. A sequential circuit has one input ***x*** and one output ***z***. and has the state diagram shown below. **[15 Points]**



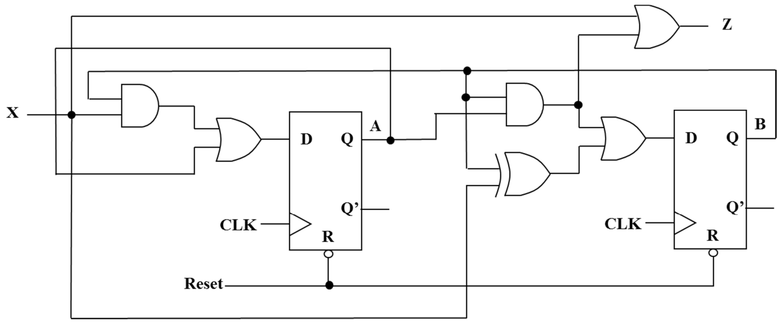
a) Design the circuit using minimum number of logic gates and positive-edge triggered D Flip-Flops. **(10 points).**

b) Using the timing diagram below, draw the output waveform ***z***. Assume the circuit starts at state **00**. **(5 points)**



Question 4. **[12 Points]**

For the sequential circuit shown below:



1. Specify the inputs, outputs, reset state, and the type (Mealy or Moore). (**2 points**)

2. Derive the state diagram of the circuit. **(9 points)**

3. Does this circuit has any unused states? Briefly explain your answer (**1 points**)

Question 5. **Label all your components, inputs, and outputs** **[8 Points]**

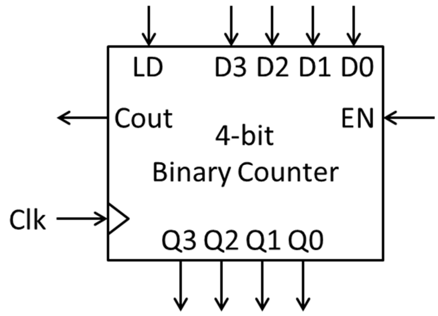
Using D flip-flop(s) and MUX(s) only (i.e., other components are not allowed), design a 4-bit register with mode selection inputs **S1** and **S0**. The register should operate according to the following table:

S1	**S0**		**Function**
0	0		No change
0	1		Parallel load (load inputs into register in parallel)
1	0		Rotate Right (i.e., shift register contents to the right feeding in the shifted bit out from the last bit location as a serial input to the first location)
1	1		Load register with 1's complement of its current content

Question 6. **[10 Points]**

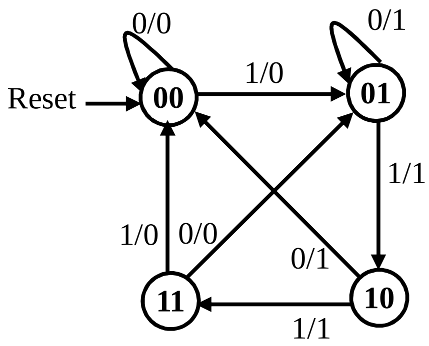
Use as many as you need of the 4-bit binary counter shown below (with the table explaining its operation) and minimal gates to design a counter that counts up from **5** to **125** in binary and then back to 5. Label properly the inputs and outputs of your designed counter.

LD	**EN**	**Operation of the counter**
0	0	Hold count
0	1	Increment count
1	X	Parallel load



Question 7. **[15 Points]**

1. The state diagram below is for a sequential circuit that one input **X** (in addition to the asynchronous Reset) and one output **Y**. Write a **behavioral** Verilog description of this circuit. **(10 points)**



2. Write a **behavioral** Verilog description of a universal register that has three control inputs in addition to the clock input; Clr, LD, and Count, **and 4-bit input Din and output Q**, with the following functionality: **(the counter does not have asynchronous inputs)** **(5 points)**

Clr	LD	Count	Functionality
0	0	0	No change (i.e. Q stay the same)
1	X	X	Clear register no matter what LD and Count are (i.e. Q=0)
0	1	X	Load the register with Din (i.e. Q=Din)
0	0	1	Count up till Q=9, then go back to 0