COE 202: Digital Logic Design
Fall 2021 – Term 211

COMPUTER ENGINEERING DEPARTMENT

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

Instructor: Dr. Muhamed Mudawar Office: 22/410-2 Phone: 4642
Office Hours: UTR 9:30 to 10:30 AM or by appointment
Course URL: https://faculty.kfupm.edu.sa/coe/mudawar/coe202/
Email: mudawar@kfupm.edu.sa

Catalog Description

Introduction to information representation and number systems. Boolean algebra and switching theory. Canonical forms: minterms and maxterms. Manipulation and minimization of completely and incompletely specified Boolean functions. Propagation delay, timing diagrams. Primitive and complex gates. Combinational circuits design. Multiplexers, decoders, encoders, comparators, adders. Sequential circuit analysis and design, basic flip-flops, clocking and timing diagrams. Registers, counters. Introduction to Verilog.

Prerequisite: PHYS 102

Course Learning Outcomes

After completing the course, you should be able to:

1. Represent numbers and perform arithmetic operations in various number systems.
2. List basic identities of Boolean algebra and perform algebraic manipulations of Boolean expressions.
3. Simplify functions using the K-map method including the use of don't care conditions.
4. Design efficient combinational circuits utilizing basic functional blocks such as adders, comparators, multiplexors, encoders, and decoders.
5. Analyze and design efficient sequential circuits using Mealy and Moore models.
6. Design registers and counters and understand their applications.
7. Model simple combinational and sequential circuits using Verilog HDL and use tools to simulate and verify correctness of design.

Textbook

Alan B. Marcovitz , *Introduction to Logic Design*, Third Edition, McGraw-Hill, 2010.

Grading

Verilog Assignments	15%	
Quizzes	15%	
Midterm Exam	30%	**Saturday, October 23, 2021, at 10 AM**
Final Exam	40%	**To be announced**

- Attendance will be taken regularly. The tenth unexcused absence results in a DN grade.
- No makeup will be made for a missing Quiz or Exam.

Week	Topics
1	• Introduction, Analog versus Digital. • Weighted number systems: decimal, binary, octal, and hexadecimal. • Number base conversion. • Representing fractions.
2	• Binary codes, BCD codes, character storage, ASCII Code. • Error detection, Parity bit. • Binary arithmetic: addition, subtraction & multiplication. • Hexadecimal addition and subtraction. Bit shifting. • Boolean algebra, truth tables, basic identities, duality principle.
3	• DeMorgan's theorem. • Algebraic manipulation and expression simplification. • Logic gates and logic diagrams. • Minterms, Maxterms, Sum-of-Minterms, Product-of-Maxterms. • Sum of Products, Products of Sums, 2-Level gate implementation.
4	• Additional gates: NAND, NOR, XOR, and XNOR. Universality of NAND and NOR. NAND-NAND and NOR-NOR implementations. Properties of XOR and XNOR. Odd and Even Functions, Parity generation and checking. • Introduction to Verilog: Verilog module, gate level modeling and gate delays, module instantiation, continuous assignment and propagation delay, writing a simple test bench.
5-6	• The Karnaugh map, two, three, and four-variable K-map • Prime Implicants and Essential Prime Implicants, Minimal SOP and POS. • Don't care conditions and simplification, multiple outputs. • Characteristics of logic gates, timing diagrams, gate and propagation delay. • Combinational circuit design procedure. • Designing a BCD to 7-Segment decoder.
7-8	• Iterative and hierarchical combinational circuit design. • Arithmetic circuits: Ripple carry adder design, carry propagation and delay analysis. • Magnitude comparator. • Signed Integers: sign-magnitude, 1's complement, and 2's complement. • Addition and Subtraction of signed 2's complement. • Design by contraction: designing an incrementer and decrementer • Unsigned versus signed arithmetic circuits.
9-10	• Functional Blocks: Decoders, Encoders, and Multiplexers • Implementing large decoders hierarchically from smaller decoders. • Function implementation using decoders. • Encoders and Priority Encoders. • Multiplexers**,** implementing multiplexers using 3-state gates. • Implementing large multiplexers hierarchically from smaller ones. • Function implementation using multiplexers. • Design Examples.

11-13	• Bit vector in Verilog, Verilog operators, module parameters, modeling adders, comparators, and multiplexers. • Behavioral description in Verilog, always block and sensitivity list, procedural assignment, if and case statements, modeling a decoder, priority encoder, and ALU. • Introduction to sequential circuits, synchronous versus asynchronous, clock cycle and frequency, latches, clocked latches, flip-flops, characteristic tables and equations. • Analysis of sequential circuits. state table, state diagram, Mealy vs. Moore, timing diagrams. • Sequential circuit design. Design procedure, state diagrams and state tables, Mealy and Moore sequence detectors, tracing state diagrams. Sequential comparator. Designing a counter with a state diagram. • Asynchronous/Direct Clear and Set Inputs. Setup, Hold, FF propagation delay. Calculating maximum clock frequency.
14-15	• Verilog modeling of D-Latch, D Flip Flop, Synchronous Set/Reset, Asynchronous Set/Reset. Verilog Structural modeling of sequential circuits, FSM modeling. • Registers, Registers with parallel load. • Shift Registers. Bi-directional shift register. Applications of shift registers. • Ripple up/down counters. • Synchronous binary counters. • Counters with Parallel load, enable, synchronous clear and asynchronous clear. • Building counters of different count. • Verilog modeling of: Parallel Load Register, Shift Register, Up-Down Counter.