COMPUTER ARCHITECTURE COE 308

QUIZ-4

Name and ID:…….

MEMORY SYSTEM

A cache has a hit time Tc=2 cycles and a miss probability Pmiss = 0.055. The main memory access time is Tmm = 36 cycles. The data-cache and instruction-cache have identical performance. A program has the following instruction distribution: probability of 0.4 for arithmetic and logic instructions, 0.2 for load, 0.1 for store, and 0.3 for control instructions. Assume control instructions do not cause any loss. The processor is running at 2 GHz.

1. Evaluate the average access time Taccess in clocks and in seconds of the memory system.

2. The processor is a five-stage MIPS processor. The ideal CPI is 5.5 clocks, e.g. assuming a hit in instruction-cache and data-cache. Evaluate the average number of clocks to process one instruction (CPI).

3. Assume a victim cache is used with Tvic = 4 cycles and a miss probability Pvic_miss = 0.5. Evaluate the average access time Taccess in clocks of the memory system when the victim cache is accessed: (1) upon a miss in the cache, and (2) simultaneously with the cache.

Solution:

1. Taccess= Tc + Pm(IC) * Tmm = 2 + 0.055 * 36= 3.98 clocks and Taccess=3.98*0.5= 1.99 ns.

2. CPI= CPI_ideal + 0.055 * (1+0.2+0.1) * 36 = 5.5+ .055 * (1+0.2+0.1) * 36 = 8.074 clocks, to account for instruction 1 fetch, 0.2 for load, and 0.1 for store.

3. In the case the victim cache is accessed upon a miss in the cache, we have Taccess = Tc + Pm * (Tvic + Pvic_miss * Tmm)= 2 + 0.055 * (4 + 0.5 * 36)=3.21 clocks. In the case of simultaneous access of victim cache with the cache, we have Taccess = Tc + Pm * ((Tvic-Tc) + Pvic_miss * Tmm)= 2 + 0.055 * ((4 -2) + 0.5 * 36)=3.1 clocks.