COMPUTER ARCHITECTURE COE 308

QUIZ-3

Name and ID:…….

Consider the (1) **MIPS** Multi-Cycle (MC) Datapath, and (2) **MIPS** Pipelined (P) Datapath.

Answer each of the following questions:

1. Suppose a benchmark program has the following instruction mix: (1) 45% of the instructions are of R-type, (2) 15% are Load, (3) 10% are Store, (4) 18% are BEQ, and (5) the rest are J-type. In the case of the P datapath we will account only of the lost cycles due to J-type instructions. Evaluate the CPI of MIPS for (1) the MC datapath, and (2) the P datapath.

   Solution: The CPI of MIPS for (1) the MC datapath is CPI = 0.45*4 + 0.15*5 + 0.1*4 + 0.18*3 + 0.12*2 = 3.73 clocks/instr. For the P datapath, the CPI= 1+ 0.12*2= 1.24 clocks/instr.

2. Determine the clock logic needed to clock the PC register in the case of (1) the MC Datapath, and (2) the P Datapath. Denote by CLK the system clock and PC clock as PC_CLK.

   Solution: The clock logic needed to clock the PC register depends on the availability of the target PC value, e.g. for Jump the target is (PC31-28, Imm24, 00) which is available at end of Decode, for Jeq and all other instructions the target is PC+4 or PC+4 +S(E(Imm-16) which is available at end of Execute. Thus, in the case of (1) the MC Datapath is PC_CLK= CLK AND (Jump: second instruction state, Jeq and all other instruction: third instr. state), and (2) the P Datapath the PC_CLK= CLK.

3. Determine the three values that must be latched by PC and which condition should be true each value. The question is to be addressed for the case of: (1) the MC Datapath, and (2) the P Datapath.

   Solution :
   For the MC Datapath, the three values are (1) Sign(Ext(imm16)) with condition (I-State=BEQ.AND.Z), (2) (PC31-28,Imm26,00) with condition (I-State=B), and PC+4 if neither of the above conditions is true. Note that I-State denotes the state value which is allocated to the instruction in the multi-cycle machine for the last state or execute phase.