جامعة الملك فهد للبترول والمعادن
King Fahd University of Petroleum & Minerals

COE301 : Computer Organization

Designing an Overflow Detector Circuit

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15 September 2013

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Designing an Overflow Detector Circuit :

- **Inputs:-**
  - A : The most significant bit of the 1st operand. (represents the sign)
  - B : The most significant bit of the 2nd operand. (represents the sign)
  - Res. : The most significant bit of the result . (represents the sign)

- **Outputs :-**

  A single bit that shows if there is an overflow or not .

- **Procedure :-**

  If the most significant bit is (0) , that means the number is +ve. However, if the most significant bit is (1) , that means the number is -ve. The overflow happens when :

  1. Adding two +ve numbers , and the result is –ve.
  2. Adding two -ve numbers , and the result is +ve.

  The truth table below shows all the cases :

A	B	Res	Overflow
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

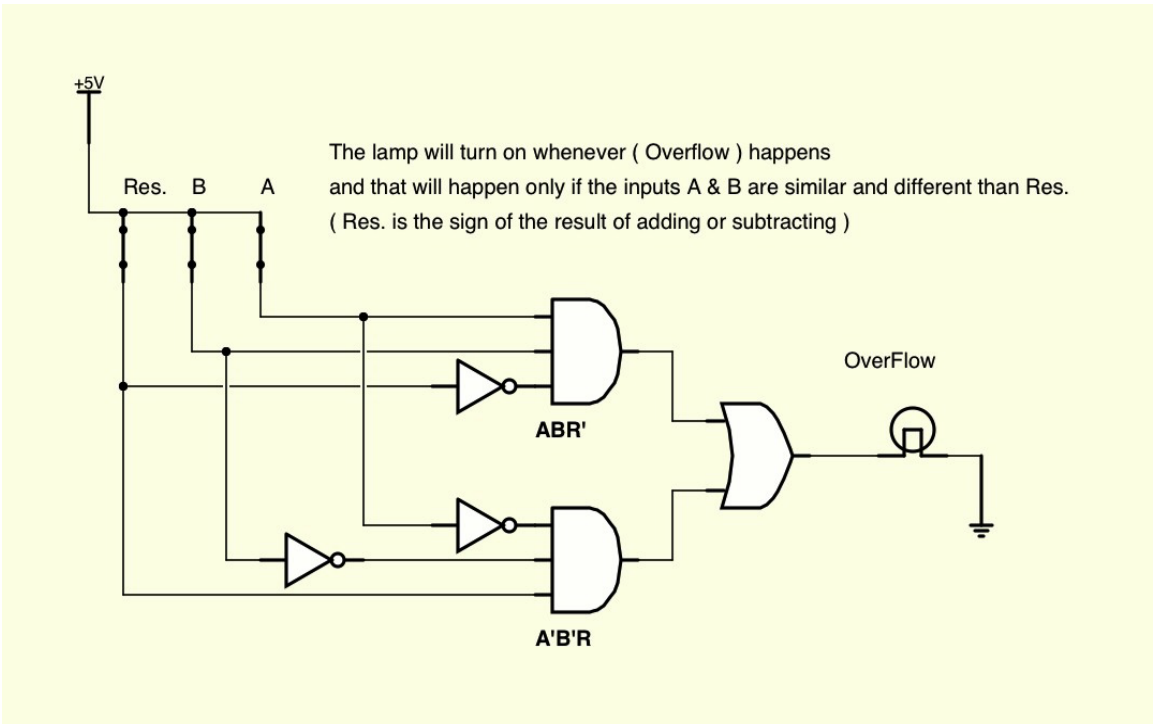
  From this truth table we can make up the K-map that will help us to design the desired circuit.

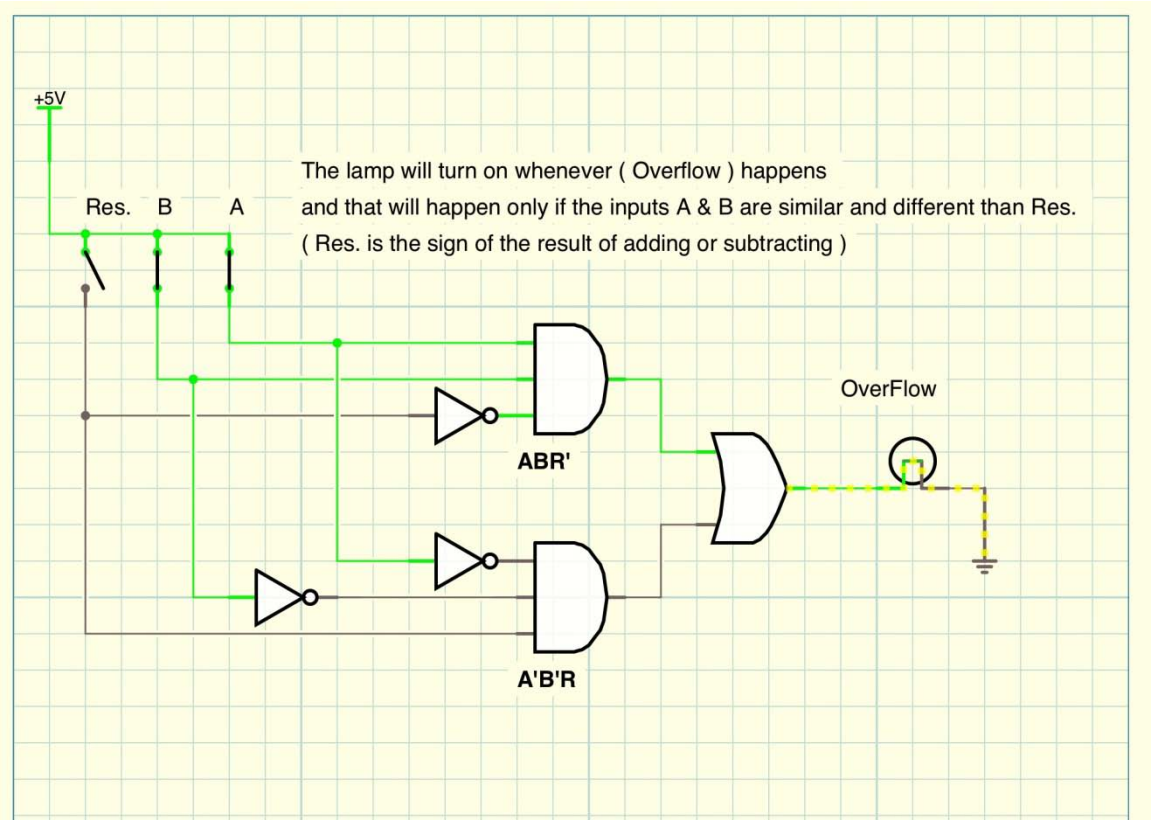
Res / AB	0	1
00	0	1
01	0	0
11	1	0
10	0	0

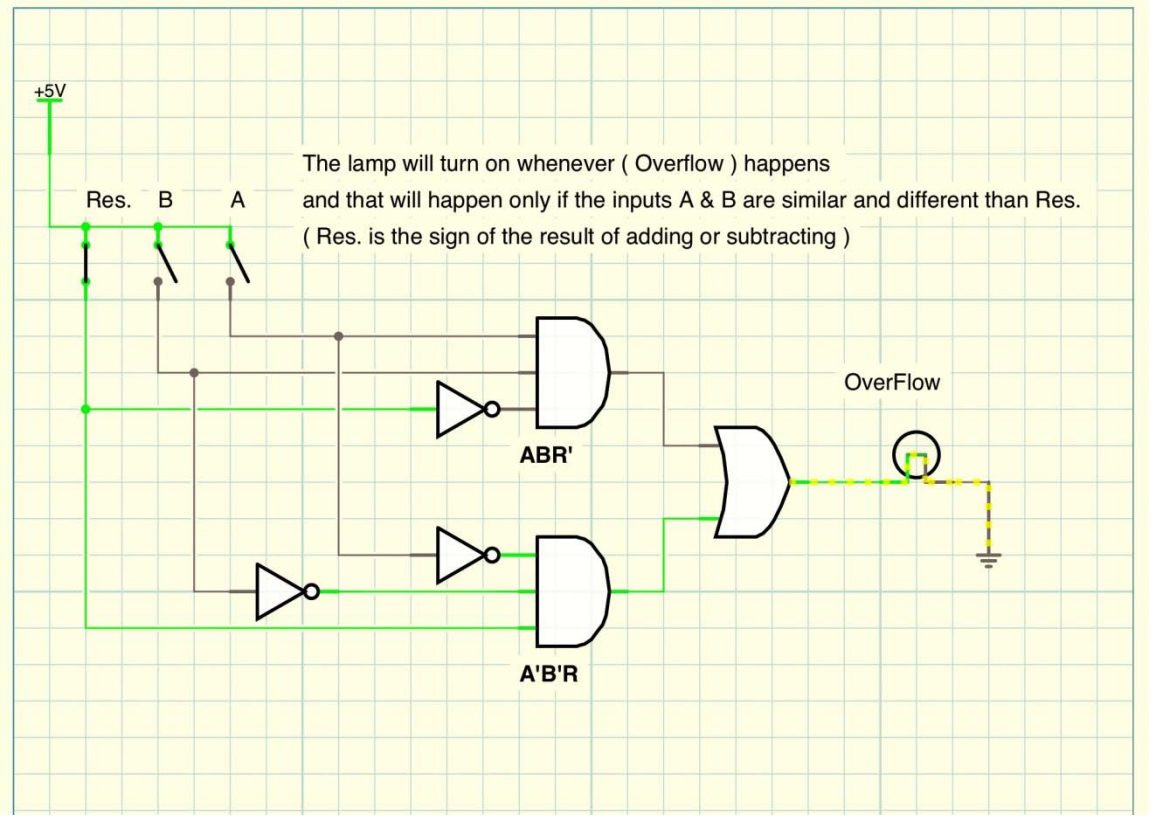
The resulting Equation that represents the K-map is :

$F = AB\bar{R} + \bar{A}\bar{B}R$

The circuit implementation is shown below. The last two pictures shows the simulation of the two Overflow cases .




+5V
Res.
B
A
The lamp will turn on whenever (Overflow) happens
and that will happen only if the inputs A & B are similar and different than Res.
(Res. is the sign of the result of adding or subtracting)
OverFlow
ABR'
A'B'R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