DIGITAL LOGIC DESIGN COE 202

QUIZ-3, Section 5

Saturday, November 29, 2008

Student Name and ID……..

Question-1: A 3-bit Carry-Look-Ahead adder

A Full-Adder (FA) has inputs A_i, B_i, and C_i and outputs $S_i = A_i$ xor B_i xor C_i and $C_{i+1} = A_iB_i + C_i (A_i$ xor $B_i)$. Answer the following questions:

1. How to modify the FA equations for the design of 3-bit Carry-look-Ahead Adder. The inputs are denoted by $A_2\ A_1\ A_0$ and $B_2\ B_1\ B_0$ with $C_0 = 0$.

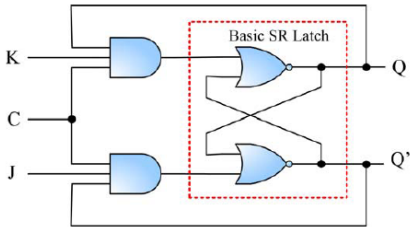
   $E_i = A_i + B_i$
   $P_i = A_iB_i$ All E and P terms take 1 gate delay.
   $S_0 = E_0$ xor C_0 take 1-gate delay.
   $C_1 = P_0$ take 1-gate delay.
   $S_1 = E_1$ xor $C_1 = E_1$ xor P_0 take 2-gate delay.
   $C_2 = P_1 + C_1\ \ E_1 = P_1 + E_1 P_0$ take 3-gate delay.
   $S_2 = E_2$ xor C_2 take 4-gate delay.
   $C_3 = P_2 + C_2\ \ E_2$ take 5-gate delay.

2. Determine the number of gate delays for getting each output S_2, S_1, S_0, and C_2.
   (see above)

Question-2: Clocked JK-Latch

Answer the following questions:

1. Give the block-diagram of the Clocked JK-Latch and show all inputs J, K, and CLK as well as outputs Q and Q'.



2. Give the characteristic table of the Clocked JK-Latch, e.g. Q+ = Function (Q, J, K)

Q(t)	J	K	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

3. Give the excitation table of the Clocked JK-Latch, e.g. (J, K) = Function (Q, Q+)

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

4. What is the reason for uncertainties in the level-triggered JK-Latch! How this problem is avoided!

   The level-triggered JK-Latch is sensitive to the clock signal level. Thus more than one transition may occur when the clock is high because some outputs are fed back to the input. The result is that the next state cannot be accurately determined. On the other hand edge-triggered memory elements (or Flip Flops) are activated only at the occurrence of the clock edge, transition from low to high or the opposite. This provides better control of the single transition that should take place.