# COE 301 COMPUTER ORGANIZATION <br> ICS 233: COMPUTER ARCHITECTURE \& ASSEMBLY LANGUAGE <br> Term 171 (Fall 2017-2018) <br> Major Exam 1 <br> Saturday Oct. 21, 2017 

Time: 120 minutes, Total Pages: 10

Name:__KEY $\qquad$ ID: $\qquad$ Section: $\qquad$

## Notes:

- Do not open the exam book until instructed
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated
- No calculators are allowed to be used in the exam

| Question | Max Points | Score |
| :---: | :---: | :---: |
| Q1 | $\mathbf{2 8}$ |  |
| Q2 | $\mathbf{1 1}$ |  |
| Q3 | $\mathbf{1 7}$ |  |
| Total | $\mathbf{5 6}$ |  |

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(Q1) Fill in the blank in each of the following questions:
(1) Assuming 12-bit unsigned number representation, the binary number 111111110000 is equal to the decimal number 4080.
(2) Assuming 16-bit signed 2`s complement representation, the hexadecimal number FEA0 is equal to the decimal number -352 .
(3) Two advantages of programming in assembly language are space and time efficiency and accessibility to system hardware.
(4) Two advantages of programming in high-level language are programs are portable and program development and maintenance are faster.
(5) The instruction set architecture of a processor consists of the instruction set, memory and programmer accessible registers.
(6) With a 24-bit address bus and 32-bit data bus, the maximum memory size (assuming byte addressable memory) that can be accessed by a processor is $\underline{2}^{24}=16 \mathrm{MB}$ and the maximum number of bytes that can be read or written in a single cycle is $\underline{32 / 8=4}$.
(7) The advantage of static RAM over dynamic RAM is that it is faster but the disadvantage is that it is less dense and more expensive.
(8) Given a magnetic disk with the following properties:

- Time of one rotation is 8 ms
- Average seek $=8 \mathrm{~ms}$, Sector $=512$ bytes, Track $=200$ sectors

The average time to access a block of 100 consecutive sectors is $\underline{8 \mathrm{~ms}+0.5 * 8 \mathrm{~ms}+100 / 200 * 8 \mathrm{~ms}=16 \mathrm{~ms} \text {. } . . . . . ~}$
(9) Assuming variable Array is defined as shown below:

Array: .word 10
.half 11,12
.byte $13,14,15,16$
The content of register $\$ \mathrm{tl}$ (in hexadecimal) after executing the following sequence of instructions is $\underline{0 x 000 \mathrm{c} 000 \mathrm{~b}}$.
la \$t0, Array
lw \$t1, 4(\$t0)
(10) The pseudo instruction bgt $\$ s 2$, 10, Next is implemented by the following minimum MIPS instructions:
slti \$at, \$s2, 11
bne \$at, \$0, Next
(11) The pseudo instruction li $\$ t 0$, $0 x 12345678$ is implemented by the following minimum MIPS instructions:
lui \$t0, 0x1234
ori \$t0, \$t0, 0x5678
(12) The pseudo instruction rol $\$ s 0$, $\$ s 0$, 4 ( $\$ s 0$ is rotated to the left by 4 bits and stored in $\$ \mathrm{~s} 0$ ) is implemented by the following minimum MIPS instructions:
srl \$at, \$s0, 28
sll \$s0, \$s0, 4
or \$s0, \$s0, \$at
(13) Assuming that $\$ \mathrm{a} 0$ contains an Alphabetic character, the instruction andi $\$ \mathrm{a} 0, \$ \mathrm{a} 0,0 \mathrm{xDF}$ will make the character stored in $\$ \mathrm{a} 0$ always upper case. Note that the ASCII code of character ' $A$ ' is $0 \times 41$ while that of character ' $a$ ' is $0 x 61$.
(14) Assume that the instruction bne $\$ t 0, \$ t 1$, NEXT is at address $0 x 00400040$ in the text segment, and the label NEXT is at address 0x00400028. Then, the value stored in the assembled instruction for the label NEXT is ( $0 \times 00400028-0 \times 00400044) / 4=F F F 9$.
(15) Assuming that variable Array is defined as shown below:

$$
\text { Array2: .half }-2,-3,4,5
$$

After executing the following sequence of instructions, the content of the two registers (in hexadecimal) is $\$ \mathrm{t} 1=000000 \mathrm{FF}$ and $\$ \mathrm{t} 2=$ FFFFFFFD.
la \$t0, Array2
lbu \$t1, 1 (\$t0)
lh \$t2, 2(\$t0)
(16) Assuming the following data segment, and assuming that the first variable X is given the address $\mathbf{0 x 1 0 0 1 0 0 0 0}$, then the addresses for variables Y and Z will be $\underline{0 \times 10010006}$ and $\underline{0 \times 10010010}$.
.data
X: .byte $10,11,12,13,14$
Y : .half $15,16,17,18$
Z: .word 19, 20
(17) To multiply the signed content of register $\$ t 0$ by 112 without using multiplication instructions, we use the following minimum MIPS instructions (HINT: 112=16*7):
sll \$t1, \$t0, 4
sll \$t0, \$t1, 3
sub \$t0, \$t0, \$t1
(Q2) Answer each of the following questions. Show how you obtained your answer:
(i) Given that TABLE is defined as: TABLE: .asciiz "Aiman El-Maleh"

Determine the content of register $\$ \mathbf{t 0}$ after executing the following code:
xor $\$ \mathrm{t} 0, \$ \mathrm{t} 0, \$ \mathrm{t} 0$
la $\$ \mathrm{t} 1$, TABLE
li \$t2, 'a'
Next: lbu \$t3, (\$t1)
beq \$t3, \$zero, ENL
ori $\$ \mathrm{t} 3, \$ \mathrm{t} 3,0 \times 20$
addi $\$ \mathrm{t} 1, \$ \mathrm{t} 1,1$
bne \$t2, \$t3, Next
addi $\$ \mathrm{t} 0, \$ \mathrm{t} 0,1$
j Next
ENL:

The content of register $\$ \mathrm{t} 0=3$ as the program counts the number of characters equal to 'A' or 'a' in TABLE.
(ii) Determine the content of register $\$ \mathrm{t} 1$ after executing the following code:

li $\$ \mathrm{t} 0,0 \times 1234$<br>xor \$t1, \$t1, \$t1<br>add \$t1, \$t1, \$t2<br>srl \$t0, \$t0, 4<br>bne \$t0, \$zero, AGAIN

AGAIN: andi $\$ \mathrm{t} 2, \$ \mathrm{t} 0,0 \mathrm{xf}$

The content of register $\$ t 1=0 x A$ as the program computes the sum of the hexadecimal digits in register $\$ \mathrm{t} 0$.
(iii) Given that TABLE is defined as: TABLE: .word 90, 70, 80, 60, 100

Determine the content of register $\mathbf{\$ v 0}$ after executing the following code:

| loop: | la | \$a0, TABLE |
| :---: | :---: | :---: |
|  | addi | \$a1, \$a0, 16 |
|  | 1w | \$v0, 0(\$a0) |
|  | addi | \$a0, \$a0, 4 |
|  | lw | \$t1, 0(\$a0) |
|  | bge | \$t1, \$v0, skip |
|  | move | \$v0, \$t1 |
| skip: | bne | \$a0, \$a1, loop |

The content of register $\$ \mathrm{v} 0=0 \times 3 \mathrm{C}=60$ as the program computes the minimum of the numbers stored in TABLE.
(Q3) Write separate MIPS assembly code fragments with minimum instructions to implement each of the given requirements. You can use pseudo instructions in your solution.
(i) [10 points] Write a MIPS code fragment that returns the maximum integer value found in a user-specified row number of a $32 \times 32$ matrix A of 32-bit signed integers. The program should read the desired row number from the user and check that it is in the range between 0 and 31. If not, the program should display the error message "Row number is out of range." and terminate. Otherwise, the program should display the message "Maximum integer in the row is" and the value of the maximum integer found in the specified row, and then terminate. Assume that matrix A is already stored in memory.

```
.data
prompt: .asciiz "Please enter a row number between 0 and 31: "
outofrange: .asciiz "Row number is out of range.\n"
outmsg: .asciiz "Maximum integer in the row is "
.text
.globl main
main:
    la $a0,prompt # display prompt string
    li $v0,4
    syscall
    li $v0,5 # read row number into $t0
    syscall
    move $t0,$v0
    bltz $t0,error # check row boundary
    addiu $t1,$t0,-31 # If $t0 > 31, then result of ($t0-31) > 0
    bgtz $t1,error
    la $t1,A # compute starting location of 1st element in desired row
    sll $t2,$t0,5 # $t2 = i*32 (ixCOL+0)
    sll $t2,$t2,2 # $t2 = i*32*4 (ixCOL+0)x(int size)
    addu $t2,$t1,$t2 # $t2 = address of 1st element in desired row
    li $t3,31 # max j = 31
    lw $t4,0($t2) # read 1st element of desired row & set as maximum
loop:
    addiu $t2,$t2,4 # increment index to point to next row element
    lw $t5,0($t2) # read next element of desired row
    ble $t5,$t4, next # next element ($t5) <= current max ($t4)?
    move $t4,$t5 # No -> set max ($t4) = next element ($t5)
next:
    addiu $t3,$t3,-1 # prepare for next row element
    bgtz $t3,loop
    la $a0,outmsg # display prompt string
    li $v0,4
    syscall
    move $a0,$t4 # output $t4 = maximum in desired row
    li $v0,1
    syscall
    j exit
error:
    la $a0,outofrange
    li $v0,4
    syscall
exit:
    li $v0,10 # exit
    syscall
```

(ii) [7 points] Given two arrays $\mathbf{A}$ and $\mathbf{B}$, write the smallest MIPS assembly fragment for the following computation. Assume that register $\$ \mathbf{s} 0$ will be used to store cnt and assume that the following registers have the mentioned values: register $\$ \mathbf{s} 1=$ number of elements, $\mathbf{N}$, in each array, register $\$ \mathbf{s} \mathbf{2}=$ base address of the array $\mathbf{A}$, and register $\$ \mathbf{s} \mathbf{3}=$ base address of the array B. Each array element is a 32 -bit signed integer. Assume that $\mathbf{N} \boldsymbol{>} \mathbf{0}$. Insert comments to clarify the meaning of instructions and the use of registers.

```
    int cnt = 0;
for (i=0; i != N; i++) {
        if (((A[i] - B[i]) > 5) || ((B[i] - A[i]) > 5)) cnt = cnt + 1;
}
```

loop:
li $\$ 50,0$
\# \$s0 = cnt = 0
lw \$t0,0(\$s2)
\# \$t0 = A[i]
lw \$t1,0(\$s3)
\# \$t1 = B[i]
addiu \$t2,\$t0,5
\# \$t2 = A[i]+5
addiu \$t3,\$t1,5 \# \$t3 = B[i]+5
bgt \$t0,\$t3,incr \# Check if (A[i]-B[i]>5)
ble \$t1,\$t2,done \# Check if (B[i]-A[i]>5)
incr:
addiu \$s0,\$s0,1 \# cnt++
done:
addiu \$s2,\$s2,4 \# point to $A[i+1]$
addiu $\$ \mathrm{~s} 3, \$ \mathrm{~s} 3,4$ \# point to $\mathrm{B}[\mathrm{i}+1]$
addiu $\$$ s1,\$s1,-1 \# decrement loop index
bne $\$$ s1,\$0,loop

## MIPS Instructions:

| Instruction | Meaning | R-Type Format |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| add \$s1, \$s2, \$s3 | \$s1 = \$s2 + \$s3 | $\mathrm{op}=0$ | rs = \$s2 | rt = \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 20$ |
| addu \$s1, \$s2, \$s3 | \$s1 = \$s2 + \$s3 | op $=0$ | rs = \$s2 | $\mathrm{t}=$ \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 21$ |
| sub \$s1, \$s2, \$s3 | \$s1 = \$s2-\$s3 | op $=0$ | rs = \$s2 | $\mathrm{t}=$ \$s3 | rd $=$ \$s1 | sa=0 | $\mathrm{f}=0 \times 22$ |
| subu \$s1, \$s2, \$s3 | \$s1 = \$s2-\$s3 | $\mathrm{op}=0$ | rs = \$s2 | $\mathrm{t}=$ \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 23$ |


| Instruction | Meaning | R-Type Format |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| and \$s1, \$s2, \$s3 | \$s1 = \$s2 \& \$s3 | op $=0$ | rs = \$s2 | $\mathrm{rt}=$ \$s3 | rd = \$s1 | sa $=0$ | 4 |
| or \$s1, \$s2, \$s3 | \$s1 = \$s2 \| \$ s 3 | op $=0$ | rs = \$s2 | $\mathrm{rt}=$ \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 25$ |
| xor \$s1, \$s2, \$s3 | \$s1 = \$s2 ^ \$ s3 | op $=0$ | rs = \$s2 | $\mathrm{rt}=$ \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 26$ |
| nor \$s1, \$s2, \$s3 | \$s1 = ~(\$s2\|\$s3) | op $=0$ | rs = \$s2 | $\mathrm{rt}=$ \$s3 | rd = \$s1 | sa $=0$ | $\mathrm{f}=0 \times 27$ |


|  | tion | Meaning | R-Type Format |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| sll | \$s1,\$s2,10 | \$s1 = \$s2 << 10 | op $=0$ | rs $=0$ | $\mathrm{rt}=$ \$s2 | rd $=$ \$s1 | sa $=10$ | $\mathrm{f}=0$ |
| srl | \$s1,\$s2,10 | \$s1 = \$s2>>>10 | op $=0$ | rs $=0$ | $\mathrm{rt}=$ \$s2 | rd = \$s1 | sa $=10$ | $f=2$ |
| sra | \$s1, \$s2, 10 | \$s1 = \$s2 >> 10 | op $=0$ | rs = 0 | $\mathrm{rt}=$ \$s2 | rd $=$ \$s1 | $s a=10$ | $\mathrm{f}=3$ |
| sllv | \$s1,\$s2,\$s3 | \$s1 = \$s2 << \$s3 | op $=0$ | rs = \$s3 | rt = \$s2 | rd = \$s1 | sa $=0$ | $\mathrm{f}=4$ |
| srlv | \$s1,\$s2,\$s3 | \$s1 = \$s2>>>\$s3 | op $=0$ | rs = \$s3 | rt = \$s2 | rd = \$s1 | sa $=0$ | $\mathrm{f}=6$ |
| srav | \$s1,\$s2,\$s3 | \$s1 = \$s2 >> \$s3 | op = 0 | rs = \$s3 | rt = \$s2 | rd = \$s1 | sa $=0$ | $\mathrm{f}=7$ |


| Instruction | Meaning | I-Type Format |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| addi \$s1, \$s2, 10 | \$s1 = \$s2 + 10 | $\mathrm{op}=0 \times 8$ | rs = \$s2 | $\mathrm{rt}=$ \$s1 | $\mathrm{imm}^{16}=10$ |
| addiu \$s1, \$s2, 10 | \$s1 = \$s2 + 10 | op $=0 \times 9$ | rs = \$s2 | $\mathrm{rt}=\$ \mathrm{~s} 1$ | $\mathrm{imm}^{16}=10$ |
| andi \$s1, \$s2, 10 | \$s1 = \$s2 \& 10 | op $=0 \mathrm{xc}$ | rs $=$ \$s2 | $\mathrm{rt}=$ \$s1 | $\mathrm{imm}^{16}=10$ |
| ori \$s1, \$s2, 10 | \$s1 = \$s2\| 10 | op $=0 \times \mathrm{d}$ | rs = \$s2 | $\mathrm{rt}=\$ \mathrm{~s} 1$ | $\mathrm{imm}^{16}=10$ |
| xori \$s1, \$s2, 10 | \$s1 = \$s2 ^ 10 | op $=0 \mathrm{xe}$ | rs $=$ \$s2 | $\mathrm{rt}=\$ \mathrm{~s} 1$ | $\mathrm{imm}{ }^{16}=10$ |
| lui \$s1, 10 | \$s1 = $10 \ll 16$ | op $=0 \times \mathrm{f}$ | 0 | $\mathrm{rt}=\$ \mathrm{~s} 1$ | $\mathrm{imm}^{16}=10$ |


| Instruction | Meaning | Format |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| j label | jump to label | $\mathrm{op}^{6}=2$ |  |  |  |
| beq rs, rt, label | branch if (rs == rt) | $\mathrm{op}^{6}=4$ | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| bne rs, rt, label | branch if (rs != rt) | $\mathrm{op}^{6}=5$ | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| blez rs, label | branch if ( $\mathrm{rs}<=0$ ) | $\mathrm{op}^{6}=6$ | $\mathrm{rs}^{5}$ | 0 | imm ${ }^{16}$ |
| bgtz rs, label | branch if ( $\mathrm{rs}>0$ ) | $\mathrm{op}^{6}=7$ | $\mathrm{rs}^{5}$ | 0 | $\mathrm{imm}^{16}$ |
| bltz rs, label | branch if (rs < 0) | $\mathrm{op}^{6}=1$ | $\mathrm{rs}^{5}$ | 0 | imm ${ }^{16}$ |
| bgez rs, label | branch if (rs>=0) | $o p^{6}=1$ | $\mathrm{rs}^{5}$ | 1 | imm ${ }^{16}$ |


| Inst | uction | Meaning | Format |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| slt | rd, rs, rt | rd=( $\mathrm{rs}<\mathrm{rt}$ ?1:0) | $\mathrm{op}^{6}=0$ | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | rd5 | 0 | $0 \times 2 \mathrm{a}$ |
|  | rd, rs, rt | rd=( $\mathrm{rs}<\mathrm{rt}$ ?1:0) | $o p^{6}=0$ | $\mathrm{rs}^{5}$ | $\mathrm{r}^{5}$ | rd5 | 0 | 0x2b |
| slti | $\mathrm{rt}, \mathrm{rs}, \mathrm{imm}{ }^{16}$ | $\mathrm{rt}=(\mathrm{rs}<\mathrm{imm}$ ?1:0) | Oxa | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |  |  |
| sltiu | $\mathrm{rt}, \mathrm{rs}, \mathrm{imm}{ }^{16}$ | $\mathrm{rt}=(\mathrm{rs}<\mathrm{imm}$ ?1:0) | 0xb | rs ${ }^{5}$ | $\mathrm{r}^{5}$ | imm ${ }^{16}$ |  |  |


| Instruction | Meaning | I-Type Format |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{lb} \quad \mathrm{rt}, \mathrm{imm}{ }^{16}(\mathrm{rs})$ | rt = MEM[rs+imm ${ }^{16}$ ] | 0x20 | rs ${ }^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| $\mathrm{lh} \quad \mathrm{rt}, \mathrm{imm}{ }^{16}$ (rs) | $\mathrm{rt}=$ MEM[rs+imm ${ }^{16}$ ] | $0 \times 21$ | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| IW $\mathrm{rt}, \mathrm{imm}{ }^{16}$ (rs) | rt = MEM[rs+imm ${ }^{16}$ ] | $0 \times 23$ | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| lbu rt, imm ${ }^{16}$ (rs) | $\mathrm{rt}=$ MEM[rs+imm ${ }^{16}$ ] | 0x24 | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| lhu $\mathrm{rt}, \mathrm{imm}{ }^{16}(\mathrm{rs})$ | $\mathrm{rt}=$ MEM[rs+imm ${ }^{16}$ ] | 0x25 | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| sb $\mathrm{rt}, \mathrm{imm}{ }^{16}(\mathrm{rs})$ | MEM[rs+imm ${ }^{16}$ ] $=$ rt | 0x28 | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| sh $\mathrm{rt}, \mathrm{imm}{ }^{16}(\mathrm{rs})$ | MEM[rs+imm ${ }^{16}$ ] $=$ rt | 0x29 | $\mathrm{rs}^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |
| sw rt, imm ${ }^{16}$ (rs) | MEM[rs+imm ${ }^{16}$ ] $=$ rt | 0x2b | rs ${ }^{5}$ | $\mathrm{rt}^{5}$ | imm ${ }^{16}$ |

## Syscall Services:

| Service | \$v0 | Arguments / Result |
| :--- | :---: | :--- |
| Print Integer | 1 | \$a0 = integer value to print |
| Print Float | 2 | \$f12 = float value to print |
| Print Double | 3 | \$f12 = double value to print |
| Print String | 4 | \$a0 = address of null-terminated string |
| Read Integer | 5 | Return integer value in \$v0 |
| Read Float | 6 | Return float value in \$f0 |
| Read Double | 7 | Return double value in \$f0 |
| Read String | 8 | \$a0 = address of input buffer <br> \$a1 = maximum number of characters to read |
| Exit Program | 10 |  |
| Print Char | 11 | \$a0 = character to print |
| Read Char | 12 | Return character read in \$v0 |

