King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 111 (Fall 2012)
Final Exam
Sunday January 15, 2012

7:30 a.m. – 10:00 a.m.

Time: 150 minutes, Total Pages: 11

Name: _____ ID: _____ Section: _____

Notes:

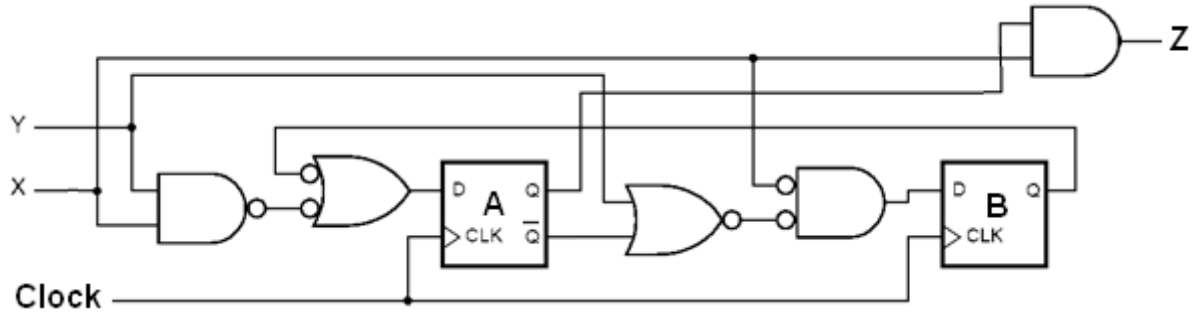
- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	20	
2	16	
3	15	
4	12	
5	27	
Total	90	

Question 1. **(20 points)**

Consider the sequential circuit below. States are AB = 00 to 11.

(*In the circuit, a bubble represents an inverter*)

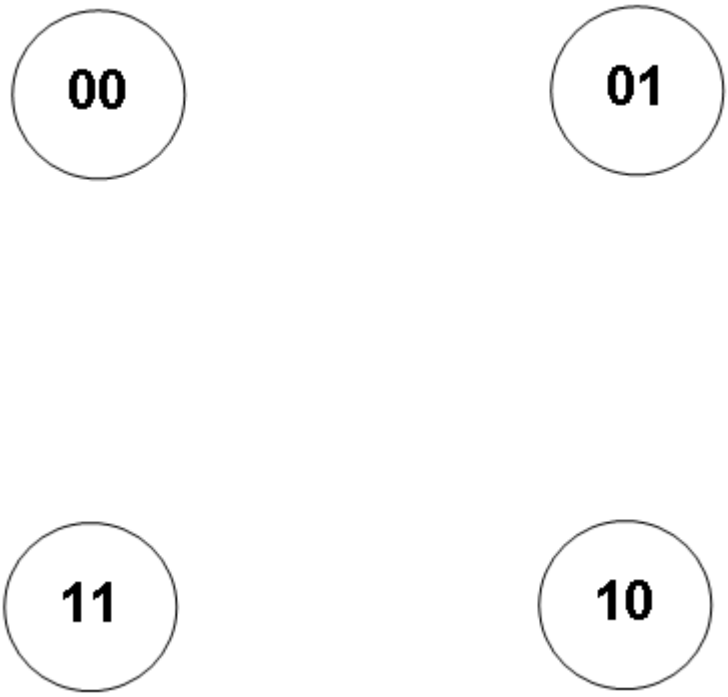


a. Is the circuit type is Mealy or Moore? (1 point)

b. Derive logic expressions for the D_A and D_B inputs of flip flops and the external output Z. (3 points)

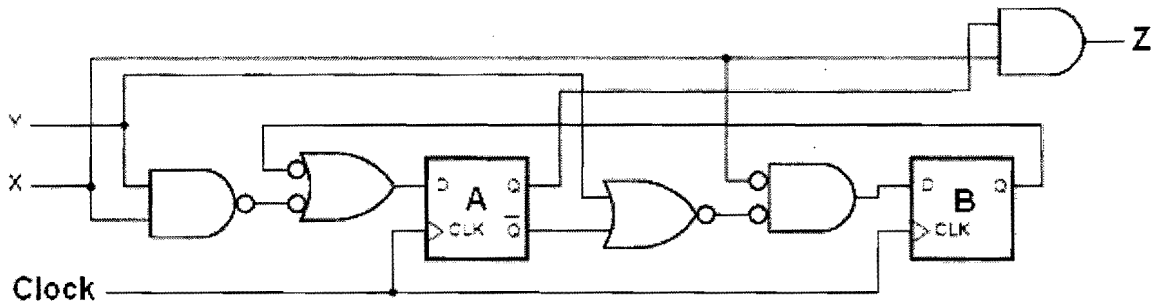
c. Provide a state table showing {present state and external inputs} and {next state and external output}. (8 points)

d. Derive a complete state diagram <u>with the states arranged as shown below</u>: (4 points)



e. The circuit can be implemented using a PROM and a register. In this case, the minimum size of the register is _____ bits, while the minimum size PROM has _____ locations (words); each being _____ bits wide. (2 points)

f. Starting at state 10, determine the minimum number of clock cycles needed to visit all remaining states only once and return to same starting state. List the sequence of states visited in the form 10 → ……. → 10. (2 points)



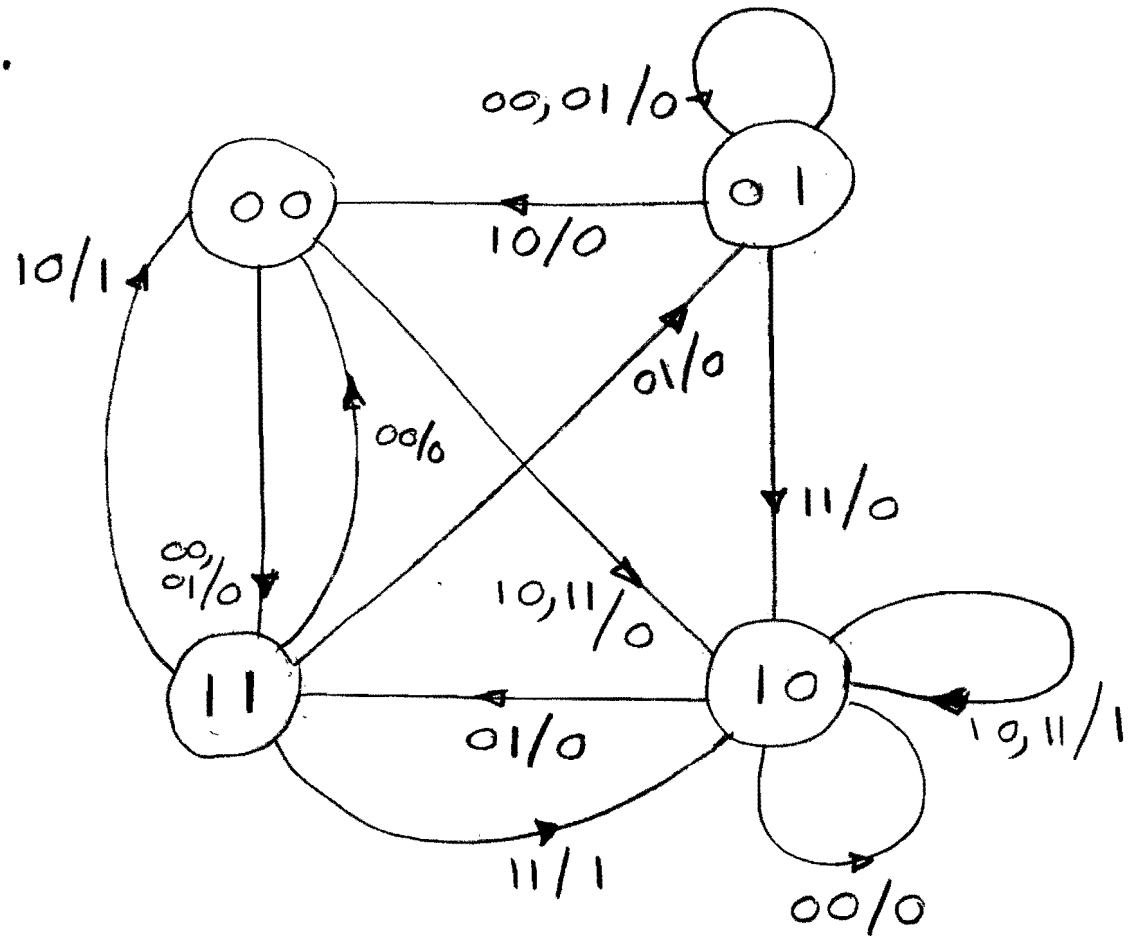
a. Mealy

b. $D_A = xy + \overline{B}$ $\quad D_B = \overline{x}\cdot(\overline{A} + y) = \overline{x}\,\overline{A} + \overline{x}y$ $\quad Z = xA$

c.

A	B	X	Y	D_A	D_B	Z
0	0	0	0	1	1	0
0	0	0	1	1	1	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	0
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	0	1	1	1	0
1	0	1	0	1	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	1	1	0	1

d.



e. The circuit can be implemented using a PROM having 16 locations (words); each being 3 bits wide and a 2-bit register of D-type flip flops.

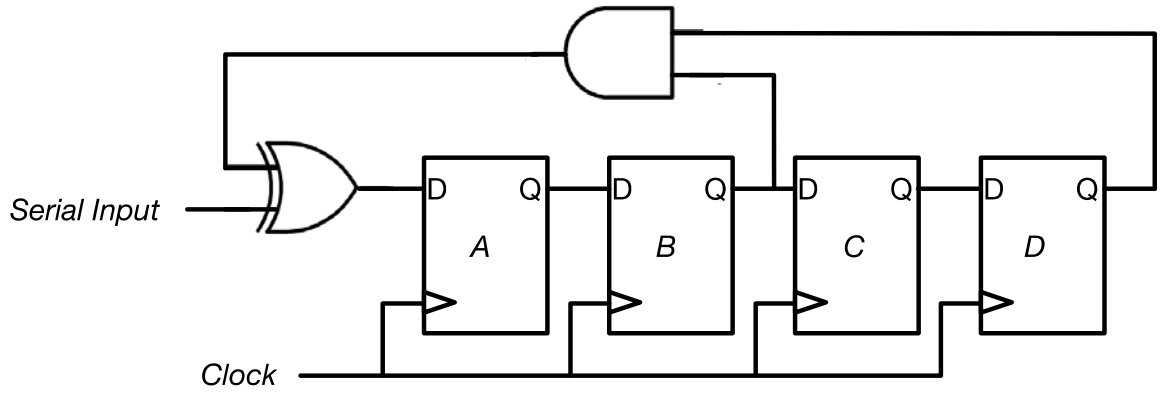
f. 4 clk cycles: 10 → 11 → 01 → 00 → 10
↑
Start

a. Question 2. **(16 Points)**

(a) (**6 points**) Using *D* flip-flop(s) and MUX(s), draw the logic diagram for an **n-bit register** with mode selection inputs S_1S_0 and a serial input S_{in}. The register should operate according to the following table:

S_1 S_0	Function to Perform
0 0	Clear the register
0 1	Hold the current contents of the register (i.e. no change)
1 0	Shift left
1 1	Load 1's complement of register contents

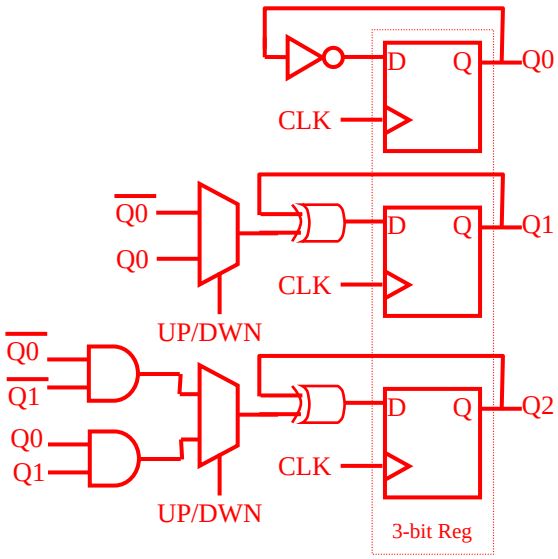
(b) (**10 points**) If the initial contents of the 4-bit shift register shown below is ABCD = 1001, fill in the entries in the table below for the given sequence of serial input. Indicate the register contents following each clock pulse. In the last column, express the register contents in hex (Stage D is the LSB).



Clock Pulse #	**Serial Input, just <u>before</u> the arrival of the next clock pulse**	**A**	**B**	**C**	**D**	**Register Contents in Hex**
Initial State	0	1	0	0	1	9
1	1	0				
2	1					
3	0					
4	0					
5						

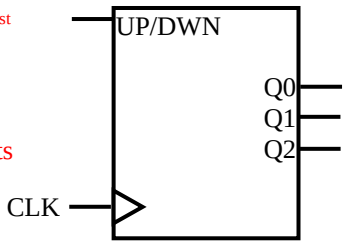
Question 3. **(15 Points)**

a) Show the implementation of modulo-8 up/down counter using **a minimum size register, MSI components** and/or any other components of your choice. When the UP/DWN input=1, then the counter counts UP and when it is 0, the counter counts downward. **(5 marks)**

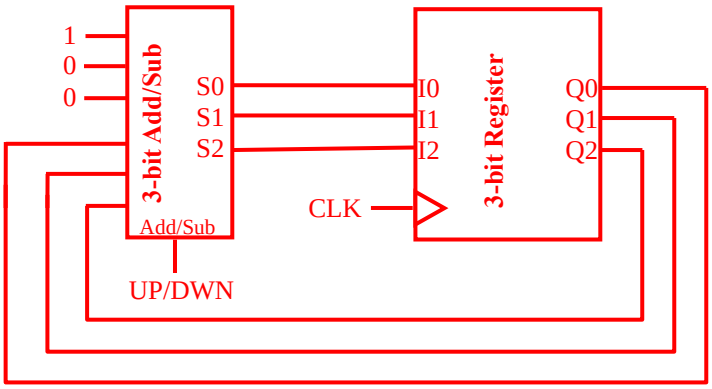


When counting Up or down, the 1st bit is always toggling (i.e. Q0+=~Q0)
For other bits, when counting UP, each bit toggles when all lower bits are 1s. e.g. Q1+=~Q1 iff Q0Q1=1

When counting Down, each bit toggle when all lower bits are 0s.
e.g.
Q1+=~Q1 iff Q0'Q1'=1

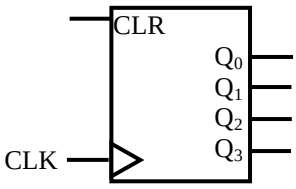


Another solution

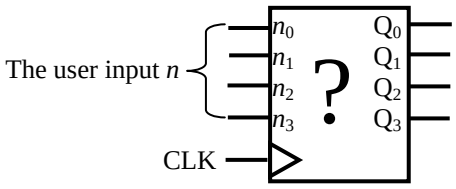


b) Using a 4-bit synchronous binary counter with synchronous clear (shown below) plus any additional components of your choice, design a modulo-*n* counter (that starts counting from 0) where *n* is a 4-bit input specified by the user as shown below.

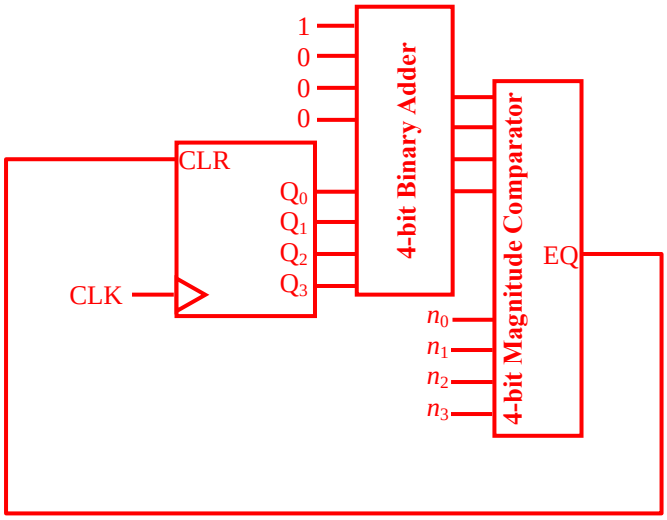
(10 marks)



The 4-bit synchronous binary counter to be used



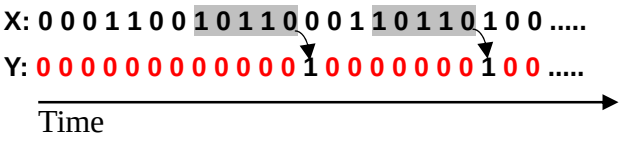
The required 4-bit selectable modulo-*n* counter



A modulo-n counter will count to n-1 then re-start from 0.

Question 4.

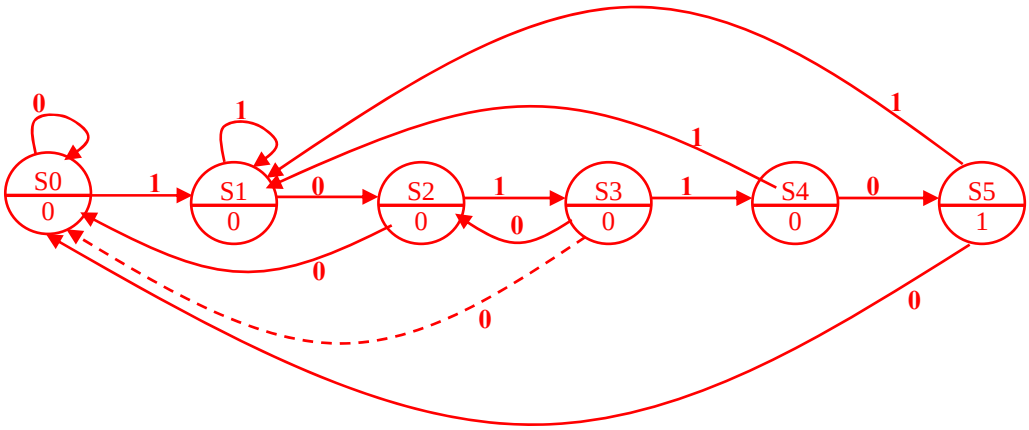
It is required to design a circuit that detects the occurrence of the following (non-overlapping) sequence of bits in an input bit stream (X): 10110, (1 followed by a zero, followed by a 1, followed by a 1, followed by a 0). When such a sequence is detected an output, Y, is set high for one clock cycle. The figure below shows an example bit stream X and the circuit's output:



a) Obtain the state diagram of this circuit as Moore Model machine **(10 marks)**

b) Specify the minimum number of FFs needed to implement this circuit and the number of unused states. **(2 marks)**

a)



b) min # of FFs = Log_2(# of states)⌉ = Log_2(6)⌉= 3 FFs – nsince we are using 3 FFs, we have 8 states → # of unused states is 2

Question 5. **(23 Points)**

(I) Shown to the right is the state transition table of a 4-state synchronous sequential circuit with a single input ***x*** and 2 outputs $\mathbf{Z_1}$, and $\mathbf{Z_0}$. The circuit also has a **RESET** input to initialize the circuit in state **00**. If the circuit is to be implemented using D-FFs, derive

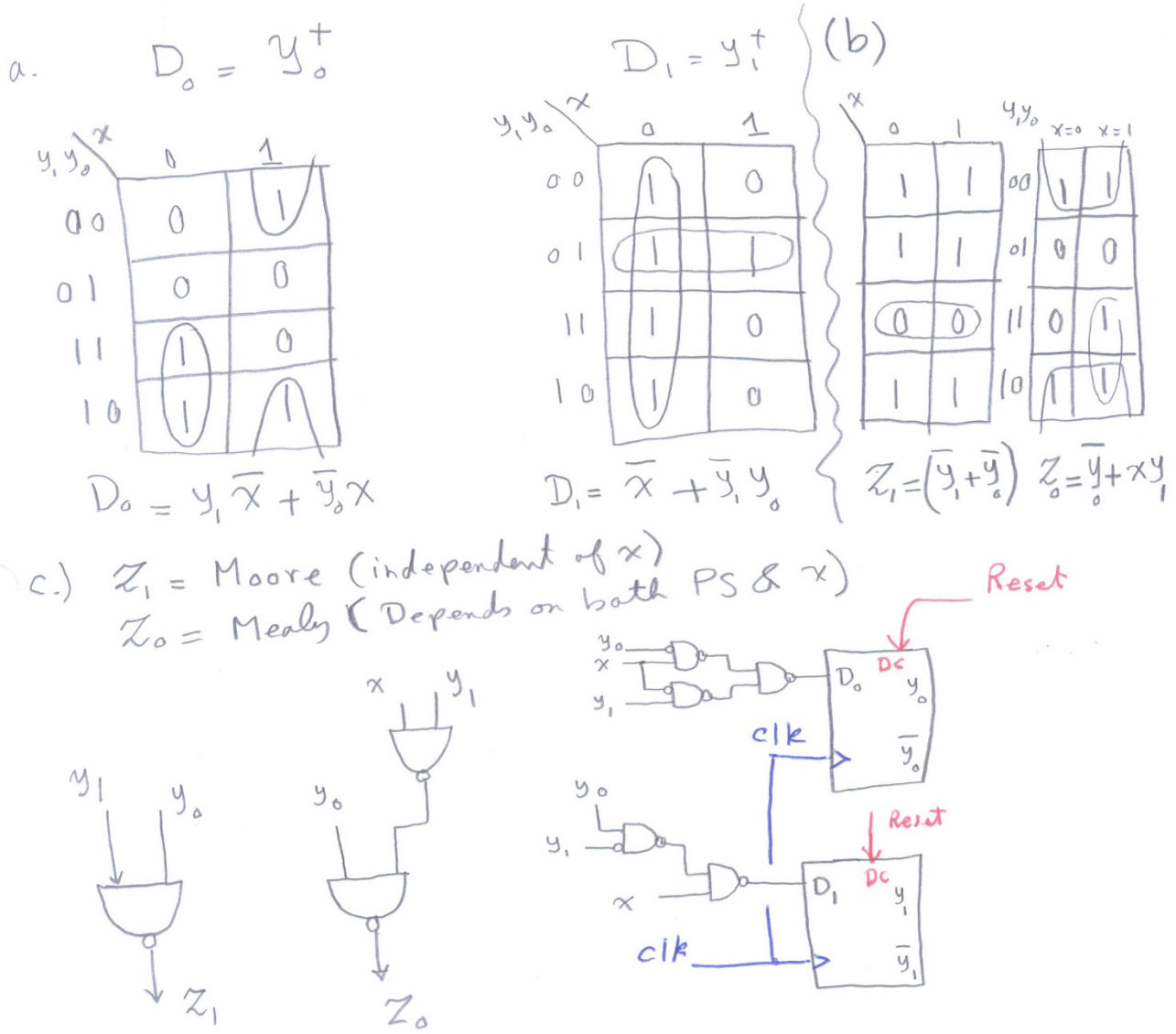
PS $(y_1\ y_0)^t$	**NS** $(y_1\ y_0)^+$ $x=0$	$x=1$	**Z_1 Z_0** $x=0$	$x=1$
0 0	1 0	0 1	1 1	1 1
0 1	1 0	1 0	1 0	1 0
1 1	1 1	0 0	0 0	0 1
1 0	1 1	0 1	1 1	1 1

a. The simplified Boolean expression of all FF inputs. (4 points)

b. The simplified Boolean expressions of the outputs Z_1, and Z_0. (4 points)

c. Classify <u>each</u> of the two outputs ($\mathbf{Z_1}$ **and** $\mathbf{Z_0}$) as either Moore type or Mealy type and **justify**. (2 points)

d. Draw the logic diagram of the circuit. (2 points)



(II)

If the shown state transition table is implemented using a single ROM and a single register:

PS* $(y_1\ y_0)^t$	**NS**** $(y_1^+ y_0^+)$ $x=0$	$x=1$	**Z_1 Z_0** $x=0$	$x=1$
0 0	0 0	0 1	0 1	1 1
0 1	0 0	1 1	1 0	0 0
1 1	0 1	1 1	1 1	0 1

* **PS = Present State**
** **NS = Next State**

i. Define the size of the required ROM, and its total capacity in bits. (**3** points)
ii. What is the size of the register in bits? (**1** Point)
iii. Give the complete ROM Table. (**2** Points)
iv. Draw the block diagram of this implementation (**You must CLEARLY LABEL each signal and each component inputs and outputs**) (**3** Points)

(i) # of Addres lines = 1 + 2 = 3 ⇒ ROM size = 2^3 location
Word size = 4 bits
ROM Capacity = $2^3 \times 4 = 32$ bits

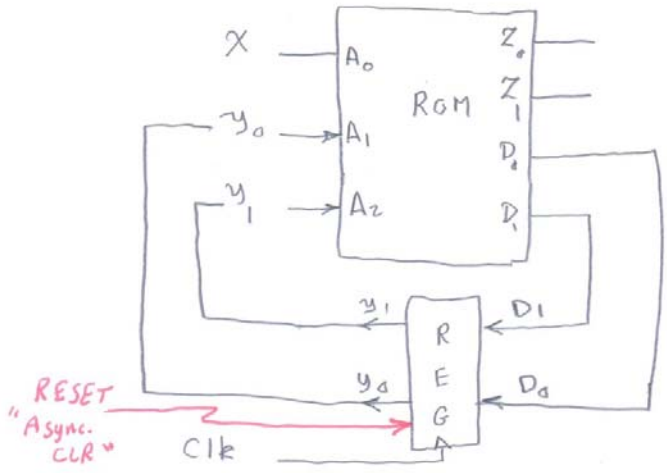
(ii) 2-bit Reg.

(iii)

ROM TABLE

Address A_2	A_1	A_0	D_1	D_0	Z_1	Z_0
0	0	0	0	0	0	1
0	0	1	0	1	1	1
0	1	0	0	0	1	0
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	1	1
1	1	1	1	1	0	1

unused stat store any values



(III)

For the same synchronous sequential circuit above assuming the initial state to be **(y_1y_0 = 01)**, draw the waveforms of y_1, y_0, Z_1 & Z_0 in response to the shown applied input on *x*. *ASSUME that the circuit uses* ***negative edge-triggered D-FFs***.

(6 Points)

PS* $(y_1 \; y_0)^t$	**NS**** $(y_1^+ y_0^+)$ $x=0$	$x=1$	**Z_1 Z_0** $x=0$	$x=1$
0 0	0 0	0 1	0 1	1 1
0 1	0 0	1 1	1 0	0 0
1 1	0 1	1 1	1 1	0 1

* **PS = Present State**
** **NS = Next State**