

King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 102 (Spring 2011)
Major Exam II
Thursday April 28, 2011

Time: 120 minutes, Total Pages: 9

Name: _____ **ID:** _____ **Section:** _____

Notes:

- Do not open the exam book until instructed
- **Calculators are not allowed** (*basic, advanced, cell phones, etc.*)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	26	
2	16	
3	12	
4	26	
5	20	
Total	100	

Question 1.

(26 points)

(A). For the following Boolean function $F(A, B, C, D) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 12, 13)$

		CD			
		00	01	11	10
AB	00	1	1	0	1
	01	0	1	1	1
	11	1	1	0	0
	10	1	1	0	1

- (i) Identify all the prime implicants and the essential prime implicants of F. (7+2=9 points)
- (ii) Simplify the Boolean function **F** into a minimal sum-of-products expression. (5 points)

(B) Consider the following Boolean function **F** together with the don't care conditions **d**

$$F(A, B, C, D) = \sum m(0, 2, 5, 8, 10), \quad d(A, B, C, D) = \sum m(1, 4, 7, 9, 11, 12, 14, 15)$$

		CD			
		00	01	11	10
AB	00	1	X	0	1
	01	X	1	X	0
	11	X	0	X	X
	10	1	X	X	1

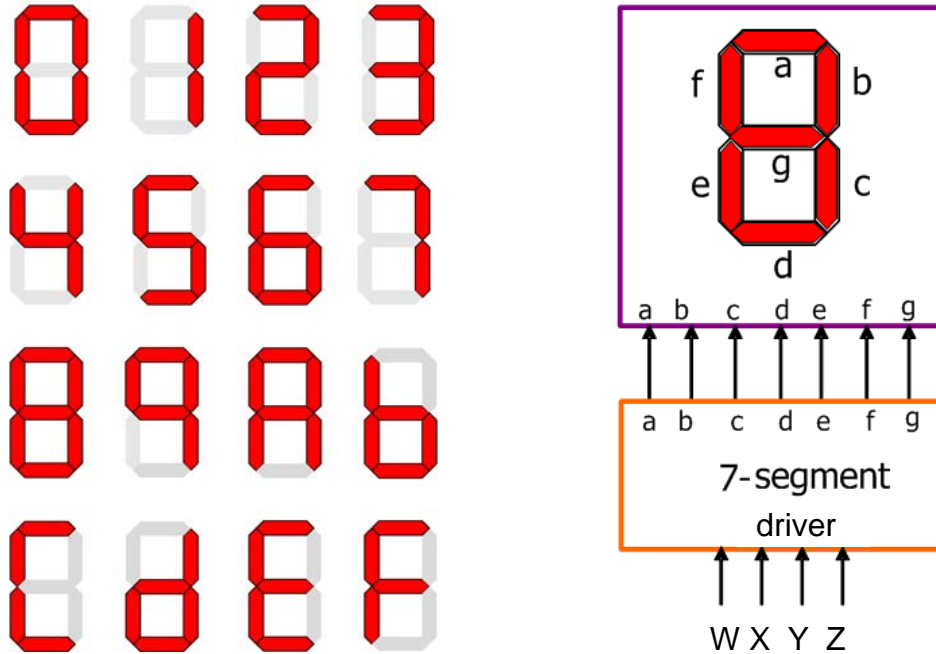
- (i) Simplify the Boolean function **F** together with the don't care conditions **d**, into minimal sum-of-products expression. (4 points)
- (ii) Starting with the sum-of-products expression, implement the function using only **NAND** gates and **Inverters**. (4 points)
- (iii) Starting with the sum-of-products expression, implement the function using only **NOR** gates and **Inverters**. (4 points)

Question 2.**(16 Points)**

Design a 3-bit decremter using only basic gates (AND, OR, and NOT). The circuit takes a 3-bit unsigned number $\mathbf{I} = \mathbf{I}_2\mathbf{I}_1\mathbf{I}_0$ as input and generates a 3-bit output number $\mathbf{Z} = \mathbf{Z}_2\mathbf{Z}_1\mathbf{Z}_0$ and a **Valid** output \mathbf{V} . Whenever $\mathbf{I} > \mathbf{0}$ the output $\mathbf{Z} = \mathbf{I} - \mathbf{1}$ and $\mathbf{V} = \mathbf{1}$. If $\mathbf{I} = \mathbf{0}$, the output is invalid which is indicated by an output $\mathbf{V} = \mathbf{0}$. Derive the simplified Boolean expressions of all outputs.

Question 3.

(12 Points)



It is required to design a 7-segment display **driver** whose input is a Hexadecimal digit such that the resulting 7-seg display is as shown above (**Note that** HEX digits larger than 9 are displayed as **A** \rightarrow **A**, **B** \rightarrow **b**, **C** \rightarrow **C**, **D** \rightarrow **d**, **E** \rightarrow **E**, **F** \rightarrow **F**). The driver circuit should generate the 7-segment control signals (a to g).

If a single **decoder** and number of **OR** gates are used to build this driver circuit;

- What is the minimum size of the decoder? (3 points)
- What is the minimum a number of OR gates required to build the 7-segment display driver circuit (3 points)
- Draw the block diagram of the circuit showing in details how the control signals **g** and **c** are generated. (6 points)

Question 4.**(26 Points)****(A)**

i. Determine the decimal value of the 7-bit binary number (1011010) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

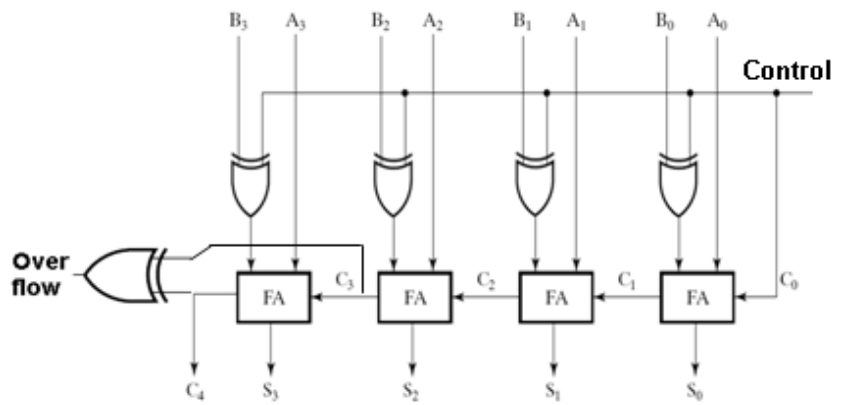
ii. Represent the decimal value (- 21) in binary using a total of 7 bits in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

iii. Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the carry values from the last two stages. For each of the three operations, check and indicate whether overflow occurred or not.

	a. $\begin{array}{r} 01101 \\ +10110 \\ \hline \end{array}$	b. $\begin{array}{r} 01010 \\ - 11001 \\ \hline \end{array}$	c. $\begin{array}{r} 11010 \\ - 00100 \\ \hline \end{array}$
Overflow Occurred? (Yes/No)			

(B) Consider the 2's complement 4-bit adder/subtractor hardware shown (FA = full adder).



i. Fill in the spaces in the table below.

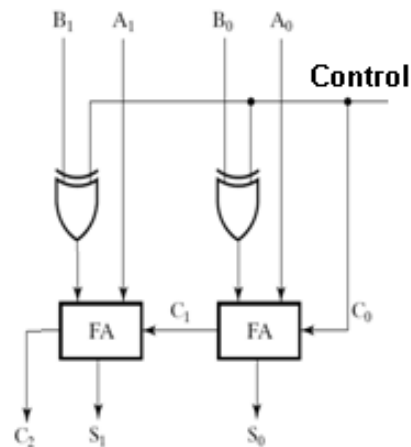
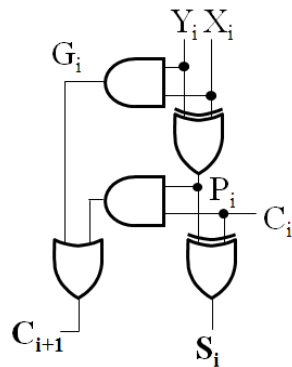
Inputs			Outputs			
A	B	Control	S (binary)	C ₄	C ₃	Overflow
0111	0101	0				
1010	1101	1				

ii. What type of 4-bit adder is used in this design? (Circle the correct answer):

- Carry-ripple adder
- Carry-look-ahead adder

(C) Consider a 2-bit version of the hardware above which is shown below. Shown also is full adder used. Given that each basic gate (i.e. AND, OR, NOT) has a delay of τ ns and the XOR gate has a delay of 3τ :

The Full Adder (FA)



i. Express, as a function of τ , the longest time interval needed for the hardware to perform an operation on the two 2-bit numbers.

ii. If such an operation must be performed in no longer than 33 ns, calculate the maximum basic gate delay allowed.

Question 5.**(20 Points)**

(A) Given the function

$$F(A,B,C) = \Pi M(0,2,4,5,6)$$

i. Implement F using one (1) 3-to-8 decoder, and one (1) **NOR** gate. Properly label all input and output lines.

ii. Implement F using two (2) 2-to-4 decoders with enable, one (1) inverter, and one (1) **OR** gate. Properly label all input and output lines.

(B) Given the function

$$F(A,B,C) = \Sigma m(1,3,7)$$

i. Implement F using an 8-to-1 MUX. Properly label all input and output lines.

ii. Implement F using a 4-to-1 MUX. Show how you obtained your solution, and properly label all input and output lines.