King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 092 (Spring 2010)
Major Exam 2
Thursday May 15, 2010

Time: 120 minutes, Total Pages: 6

Name:_____ ID:_____ Section: _____

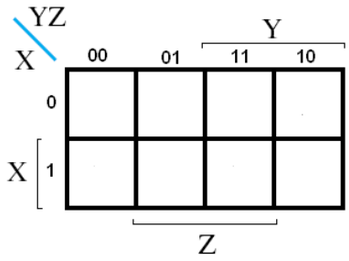
Notes:

- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1		
2		
3		
4		
Total		

Question 1. **(xx points)**

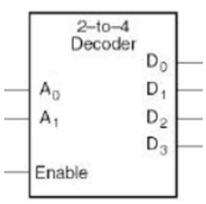
1. **Fill in the Spaces:** (Show all work done to reach your answer)



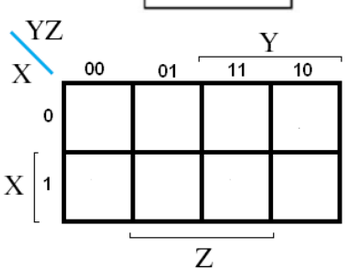
a. Using the K-map opposite, the function $F(X, Y, Z) = \overline{X}\overline{Z} + XY\overline{Z} + X\overline{Y}\overline{Z}$ simplifies to _____ (1 literal). Show your work on the map.

b. The symbol  is an equivalent representation of a _____ gate.

c. $F(X, Y, Z) = \overline{X \oplus Y \oplus Z}$ is _____(0/1) for XYZ = 110. This function can be used to generate and detect _____ even/odd parity in digital communications.



d. The 2-to-4 decoder with Enable shown opposite can be used as a _____-to-_____ demultiplexer, with the data to be demultiplexed applied to the _____ input.

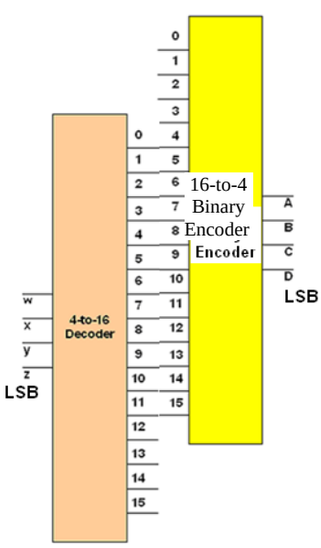


e. On the K-map opposite, mark the 1s of the following function:

$F(X, Y, Z) = (\overline{X} + \overline{Z}).(Y + Z).(X + Y + \overline{Z})$

f. For the code converter shown opposite, fill in the spaces in the following table:

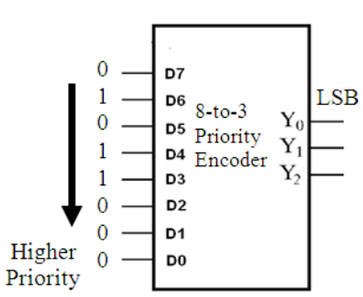
Input Code (wxyz)	Output Code (ABCD)
0110	
	1101



g. In the ripple carry adder, a carry generated from a given stage always leads to a carry from the next stage: _____(True/False).

h. Carry-look ahead adders perform addition faster than ripple carry adders: _____(True/False)

i. With the indicated input, the priority encoder shown opposite produces the binary output $Y_2Y_1Y_0$ = _____.



Question 2. **(xx Points)**

2.1 We would like to design a combinational circuit that takes as input a 3-bit unsigned binary number **X** and produces an output **Y** where $\mathbf{Y} = \mathbf{X}^2$.

a. How many bits are needed to represent the circuit output?

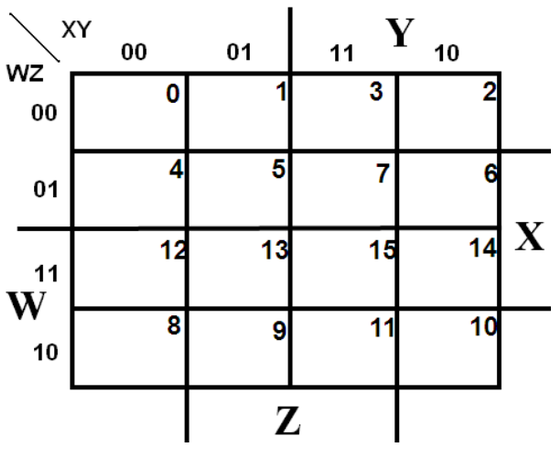
b. Provide the truth table for the circuit, showing the bits of the inputs and outputs, with the MSB on the left in each case.

2.2 Given the function $F(W, X, Y, Z) = \sum m(1,3,5,6,7,9,11,14)$

a. Plot the function on the K-map opposite, showing both the 1s and 0s of the function.

b. Express F as a minimized sum of product

c. Express F as a minimized product of sums

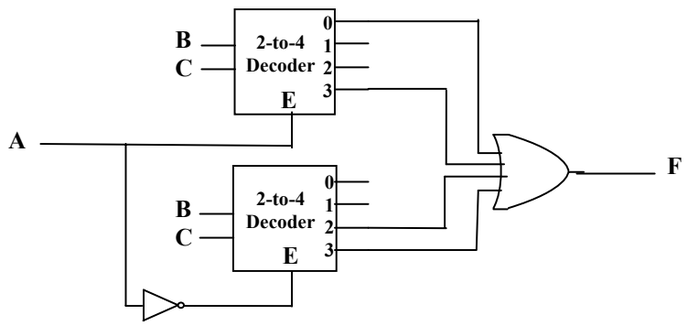


d. Draw the logic diagram for a 2-level implementation of the result in (b) above using only one type of universal gates. Assume that both true and complemented forms of each variable are available.

Question 3. **(xx Points)**

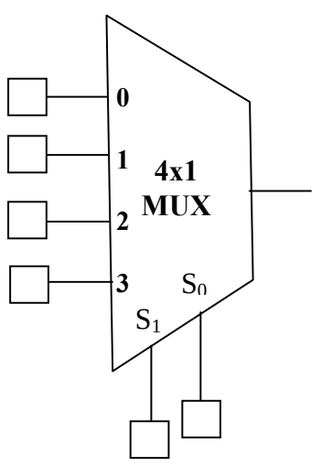
a. Analyze the circuit shown below and express F as a sum of minterms:

F (A,B,C) = ∑m ( )



b. The truth table of a combinational function F is shown below. Implement F using a 4x1 MUX (*Use A, B as selection lines*). Clearly label every input of the multiplexer.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



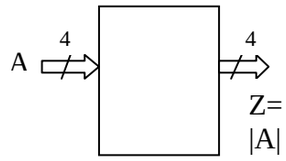
Question 4. **(xx Points)**

- In this question, you ***may ONLY use any number of the following parts*:**

  Inverters, 4-bit Binary Parallel Adders, Decoders , Encoders, Multiplexers, 4-bit Magnitude Comparators, Half Adders, and Full Adders.

- You must CLEARLY LABEL the MSI part used together with ALL INPUTS & OUTPUTs.

a. Given a 4-bit **signed 2's complement number A**, design a circuit which outputs a 4-bit unsigned number **Z** which is equal to the magnitude of **A**, i.e. **Z= |A|**



b. Given FOUR 4-bit numbers **W, X, Y, and Z:**

i. If **S = W + X + Y + Z**, what is the size of S (in bits)

ii. Design a circuit that computes **S,** using **only *any of the above listed parts*.**