King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Digital Logic Design (T161)

Verilog Assignment # 02 (*due date & time: Thursday 22/12/2016 during class period*)

Using a Verilog simulator, build a **behavioral code** and a **testbench code** for a circuit that takes two 4-bit unsigned binary numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ and a 2-bit user selection input $S = S_1S_0$. The circuit should produce a 5-bit output $O = O_4O_3O_2O_1O_0$ according to the following table:

S_1S_0	O is equal to
00	Max(A, B)
01	Min(A, B)
10	$2 \times A$
11	$\lvert A - B \rvert$ (i.e. absolute value of $(A - B)$)

Simulate the circuit for the 4-bit binary equivalent of each of the following eight test cases with 10 time units of separation between one test case and the next test case:

1. **A = 14, B = 5, S_1S_0 = 00**
2. **A = 14, B = 5, S_1S_0 = 01**
3. **A = 14, B = 5, S_1S_0 = 10**
4. **A = 14, B = 5, S_1S_0 = 11**
5. **A = 5, B = 14, S_1S_0 = 00**
6. **A = 5, B = 14, S_1S_0 = 01**
7. **A = 5, B = 14, S_1S_0 = 10**
8. **A = 5, B = 14, S_1S_0 = 11**

Save your behavioral code and testbench code and an image of the timing diagram results as a Word document and name the file "*Verilog02_yourStudentID.doc*".

Deliverables:

1. Send a soft copy of your Word file to both myself (marwan@kfupm.edu.sa) and the grader (s201381710@kfupm.edu.sa) with the "subject" line being "*COE202-Verilog02-yourStudentID*".
2. Submit a printout (i.e., hard copy) of your Word file. Make sure that both the sets of inputs and the sets of outputs show up in the timing diagram results printout.

IMPORTANT: The behavioral testbench codes and the timing diagram results developed and submitted should be the result of **your own individual genuine effort**. I follow a zero tolerance policy regarding plagiarism.