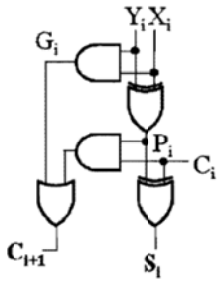
King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 – Digital Logic Design (T121)

Homework # 04 (*due date & time: Saturday 17/11/2012 during class period*)

***** Show all your work. No credit will be given if work is not shown! *****

Problem # 1 (20 points): The Full-Adder circuit is shown to the right. Given the following gate delays;



Gate/ Circuit	Propagation Delay
Inverter	**1 τ**
AND, OR	**2 τ**
XOR	**4 τ**

(i) **(5 points)** What is the **carry** propagation delay per Full adder stage?

(ii) **(15 points)** For an ***n*-bit** Ripple-Carry **Adder-Subtractor**, what is the total delay for the n^{th} sum bit and the $(n+1)^{th}$ carry-out bit?

Problem # 2 (20 points): Use a 4×16 **non-inverted-output decoder** and external gate(s) to implement the following function:

$$F(A,B,C,D) = \sum(1,3,5,8,10,14)$$

Problem # 3 (20 points): Repeat problem # 3 but use a **4×16 inverted-output decoder** and external gate(s).

Problem # 4 (20 points): Repeat problem # 3 but use a **16×1 MUX** and external gate(s).

Problem # 5 (20 points): Repeat problem # 3 but use an **8×1 MUX** and external gate(s). Connect ***C, A,* and *D*** to S_2, S_1, and S_0, respectively.