King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 202 Fundamentals of Computer Engineering (3-0-3)

Instructor: Dr. Marwan Abu-Amara
Office: 22-145
Phone: 1632
E-mail: marwan@kfupm.edu.sa
Term: 102 (2nd term 2010–2011)
Day & Time: SMW 10:00 AM – 10:50 AM
Location: 24-120
Textbook: *Logic and Computer Design Fundamentals,* Morris Mano and Charles Kime, Fourth Edition, Prentice Hall International, 2008.
Office Hours: SMW 11:00 AM – 11:50 AM (or by appointment)
Web Site: http://faculty.kfupm.edu.sa/COE/marwan

Tentative Grading Policy:
- Homeworks   **10%** (Each homework may carry a different weight)
- CAD Assignments   **5%** (Each CAD assignment may carry a different weight)
- Quizzes   **10%** (Each quiz may carry a different weight)
- Major Exam I   **20%** (Thursday March 17, 2011)
- Major Exam II   **25%** (Thursday April 28, 2011)
- Final Exam   **30%** (Saturday June 4, 2011 – 7:30 AM)

IMPORTANT NOTES:
- All KFUPM regulations and standards will be enforced. Attendance will be checked each class. The KFUPM rule pertaining to a DN grade will be strictly enforced (i.e. **> 9 absences** will result in a DN grade). *Check your university e-mail regularly for warnings regarding your absences.*
- If you are late to the class for <u>more than 5 minutes</u> (i.e. arrive after 10:05 AM), you will **NOT be allowed to enter** the classroom and you will be considered absent for that class.
- Only university approved/certified excuses will be accepted, and should be presented **no later than 1 week** after absence.
- Use of cell phones and PDAs during class period and during exams is absolutely **prohibited**.
- Homeworks are to be submitted **in class** on the due date during the class period. Late homeworks will **NOT be accepted**.
- You have 48 hours to object to the grade of a homework, a quiz, or a major exam from the end of the class time in which the graded papers have been distributed back. If for some reason you cannot contact me within this period, send me an email requesting an appointment. The email should be sent within the 48-hour time period.
- **NO make up exams**. ALL homeworks and quizzes will be counted towards your grade.
- Final exam is **<u>comprehensive & common</u>**.

Tentative schedule:

Week	Topics	Ref.
1	• Introduction: Information processing, and representation, Digital vs Analog quantities, Number systems: Binary system • Weighted Number Systems: Decimal, Binary, Octal and Hexadecimal • Arithmetic in Binary and Hex (addition, subtraction, multiplication) • Number base conversion (Dec to Bin, Oct, and Hex, General) • Conversion (Bin, OCT, Hex)	1.1 1.2 1.3 5.3 5.4
2	• Number base conversion (Bin, OCT, Hex) • Machine Representation of Unsigned & Signed Numbers: sign-magnitude, 1's complement, and 2's complement • Signed Binary Arithmetic. (Addition and Subtraction) • Decimal Codes: BCD, Excess-3, other codes, BCD Arithmetic, Parity Bits	5.3 5.4 1.3 3.10 1.4
3	• Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra, Principle of duality • Basic identities of Boolean algebra, DeMorgan's law, Algebraic manipulation • Algebraic manipulation: Absorption, Consensus	2.1 2.2 2.2
4	• Complement of a function • Canonical and Standard forms, minterms, Maxterms, SOP, POS • Physical properties of gates: fan-in, fan-out, propagation delay, timing diagrams, Tri-state drivers	2.2 2.3 2.9
5	• *Map method of simplification*: 2-variable and 3-variable K-Map • Implicants, Prime Implicants, Essential Prime Implicants • *Map manipulation:* Simplification procedure. 4-variable K-map • SOP and POS simplification	2.4 2.5 2.6
6	• Don't care conditions and simplification • 5-variable and 6-variable K-map simplification • *Implementation using NAND and NOR gates:* 2-level & Multilevel • Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking	2.5 2.7
7	• Combinational Circuit Design Procedure & Examples: Code Converter, BCD to 7-Segment Display Conversion, Magnitude Comparator, Half and Full Adders, Ripple Carry Adder design	2.8 3.1 3.3
8	• Combinational Circuit Design Procedure & Examples: Carry Look-ahead adder, Binary Adder-Subtractor, BCD Adder	3.3, 5.1-5.4
9	• Decoders 2x4, 3x8, 4x16. Designing large decoders from smaller decoders • Function implementation using decoders • Encoders: Priority Encoders. Applications of decoders and priority encoders • Multiplexers: 2x1, 4x1. Constructing large MUXs from smaller ones • Function implementation using multiplexers	5.2 5.6 4.3 4.6
10	• MSI Design Examples • *Sequential Circuits:* Latches, Clocked latches: SR, D, T and JK. • *Flip-Flops:* Master-Slave, D-FF • Designing flip-flops from other flip-flops	4.4-4.6 4.4-4.6 5.6, 6.1, 6.2
11	• *Asynchronous/Direct Clear and Set Inputs.* Setup, Hold, FF propagation delay • *Sequential Circuit Design.* Design procedure, state diagrams and state tables • Analysis of Sequential Circuits, state table, state diagram • Registers, Registers with parallel load	6.2 6.3 6.6
12	• Synchronous Binary Counters: Up-Down Counters • Counters with Parallel load, enable, synchronous clear and asynchronous clear • Use of available counters to build counters of different count • Design with unused States • Shift Registers. Bi-directional shift register	6.6 6.4
13	• Mealy vs. Moore machine • Design Examples and Calculation of maximum clock frequency	6.5
14	• Memory devices: RAMs & ROMs • Combinational Circuit Implementation with ROMs • Sequential Circuit Implementation using ROMs	6.4, 6.5 7.1 7.6
15	• Programmable Logic Devices: PLAs, PALs, FPGA'a • *Review*	7.6, 3.6 3.6

Course Learning Outcomes Table

Course Learning Outcomes	Outcome Indicators & Details	Assessment Methods & Metrics	Min. Weight	ABET 2000
1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.	➢ Represent integer and fractional values in various number systems ➢ Convert number representation from one system to another ➢ Perform arithmetic operations in various number systems ➢ Represent data in different binary codes including error detecting codes ➢ Simplify Boolean expressions using Boolean algebra & identities	➢ Assignments ➢ Quizzes ➢ Exams	20%	A (H)
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.	➢ Derive gate-level implementation of a given Boolean expression and vice versa ➢ Ability to build larger combinational functions using predefined modules (e.g., decoders, multiplexers, adders, Magnitude comparators.) ➢ Ability to build a state diagram / table for both Moore & Mealy models from functional description ➢ Ability to design & implement Moore & Mealy model synchronous sequential circuits using different Flip-Flop types. ➢ Ability to draw timing diagrams for major signals of both sequential and combination circuits	➢ Assignments ➢ Quizzes ➢ Exams	50%	C (H)
3. Ability to use CAD tools to simulate and verify logic circuits.	➢ Ability to simulate and verify the operation of combinational circuits ➢ Ability to simulate and verify the operation of sequential circuits	➢ Assignments	5%	K (L)

ABET 2000 COE Program Learning Outcomes

(a) an ability to apply knowledge of mathematics, science, and engineering
(b) an ability to design and conduct experiments, as well as to analyze and interpret data
(c) an ability to design a system, component, or process to meet desired needs
(d) an ability to function as an effective team member
(e) an ability to identify, formulate, and solve engineering problems
(f) an understanding of professional and ethical responsibility
(g) an ability to communicate effectively
(h) the broad education necessary to understand the impact of engineering solutions in a global and societal context
(i) a recognition of the need for, and an ability to engage in life-long learning
(j) knowledge of contemporary issues
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice
(l) Knowledge of Probability and Statistics and their applications in Computer Engineering
(m) Knowledge of Discrete Mathematics
(n) The ability to design a system that involves the integration of hardware and software components