# A CONTENTION-FREE DOMINO LOGIC FOR SCALED-DOWN CMOS TECHNOLOGIES WITH ULTRA LOW THRESHOLD VOLTAGES

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## ABSTRACT

A new contention-free Domino logic (**CF-Domino**) that is especially suited for low threshold voltage (LVT) is reported. Its superior noise margin and speed over conventional Domino circuits for LVTs are demonstrated using **HSPICE**® simulations and a 0.25μm CMOS technology with a supply voltage of 2.5V. The impacts of the new technique on dynamic and leakage powers and area are also presented.

## I. INTRODUCTION

Since the emergence of dynamic CMOS gates (DOMINO) [1], shown in Figure 1, they became the main option for implementing high-speed logic paths. Their speed and area advantage over static CMOS circuits [2] makes them indispensable for high performance applications such as microprocessors. However, as the chips' power grew up, lowering the supply voltage has emerged as the most favorable way of reducing the power [3]. To prevent speed degradation, threshold voltages had to be lowered as well, which in turn increased the leakage currents. While the increased leakage does not affect the functionality of static CMOS, it reduces the noise margins (NM) of dynamic circuits and ultimately causes their failure. Dual Vt (DVT) technologies were proposed as a solution to this problem [4], where LVT devices are used in static CMOS gates and high Vt (HVT) devices used in Domino gates. This option not only is more expensive than the single Vt option, but it deprives the Domino gates from benefiting from the higher speed of the LVT devices, thus reducing the Domino's speed advantage. Also, as it was clearly demonstrated in [4], for the same channel length, it is not possible to optimize two devices with two different Vts. This means that the HVT device would have a more compromised performance than a similar device in a single Vt technology, further degrading the Domino's performance. All this makes it very difficult for products to meet their speed targets as the technology and supplies scale down. Another recent dual Vt implementation of Domino focused on reducing the leakage while reaping the speed advantages of LVT devices [5]. However, no attention was paid to noise margins. This is very impractical since Domino is especially vulnerable to noise.

In this work, a modified Domino gate (**CF-Domino**) is proposed to resolve the trade-off between speed and NM and extend the Domino's operation into the deep LVT regime. The trade-off between NM and speed for the conventional Domino is first demonstrated as a function of Vt and then the performance of the CF- Domino circuit is presented.

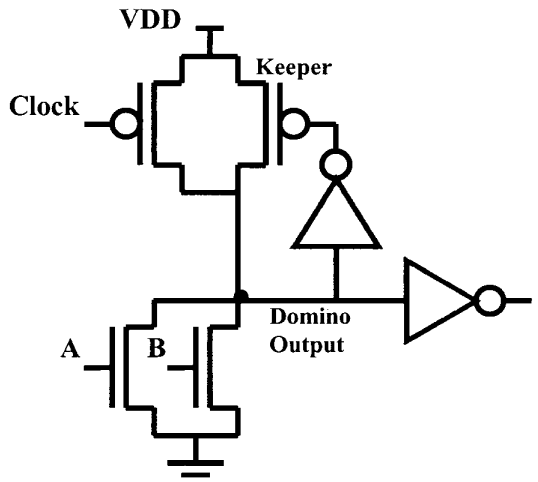


**Figure 1: A 2-input conventional Domino NOR gate.**

## II. CONVENTIONAL DOMINO

Referring to Fig.1, the conventional Domino operates as follows. During the pre-charge phase (when clock is low), the Domino output is pre-charged to VDD and the keeper is turned **ON**. When the clock goes high (evaluation phase), depending on the inputs, the Domino output is either discharged to GND or remains high at VDD. If all inputs are low, the keeper will keep the output high despite any existing noise. So the larger the keeper width ($\mathbf{W_{keeper}}$), the better the NM. When at least one of the inputs is high, the output is pulled low and the keeper is turned **OFF**. The larger the keeper, the larger the contention that occurs between the pulling down NMOS device and the keeper and the slower the gate. This is the basic speed-NM trade-off of the conventional Domino. This trade-off becomes severer at lower Vts because of the increased NMOS leakage. Figure 2 shows the voltage waveforms of a Domino gate. It shows

0-7803-5482-6/99/$10.00 '2000 IEEE

how the Domino output starts switching while the keeper is still **ON** (the contention).

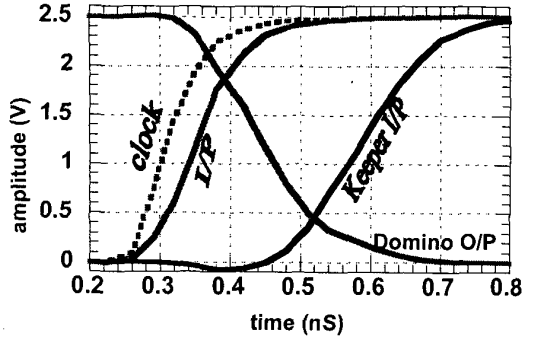


**Figure 2: The waveforms of a conventional Domino gate.**

Figure 3 shows the DC characteristics of an 8-input conventional Domino NOR gate for several Vt keeping the keeper size constant and tying all inputs together. An 8-input NOR was chosen because Domino is mostly favored for wide $\mathbf{Fan_{In}}$ NOR gates and these represent the worst case scenario for leakage-induced noise margins degradation. The figure shows how the low NM decreases as Vt decreases.

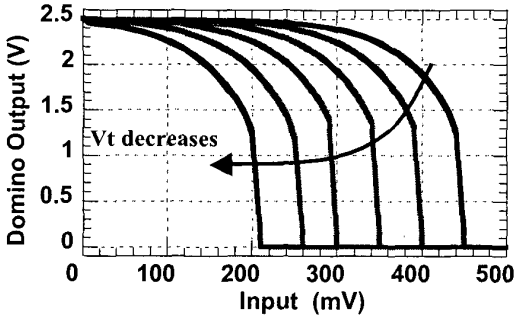


**Figure 3: The DC characteristics of Domino as a function**

Figure 4 shows the normalized delay of a 3-stages chain of 8-input Domino NOR gates with a $\mathbf{Fan_{Out}}$ of 3 versus Vt for two cases; constant NM (by varying the keeper's size) and constant keeper size (i.e. variable NM). The normalized keeper size for the constant NM case is also shown on the same graph. The NM was defined according to the criterion in [4], the input voltage above ground that causes a 10% drop from VDD at the Domino output. The NM was set to 10% of VDD. This figure shows the trade-off between NM and speed as Vt is reduced. In order to keep the NM of the Domino gate constant, the keeper size had to be increased. This, in turn reduced the speed gain at lower Vts and eventually increased the delay. The constant keeper curve shows the maximum possible gain in speed with lowering the Vt. However, in the case of conventional Domino, this can only be achieved if the reduction in the NM with Vt was wrongfully ignored.

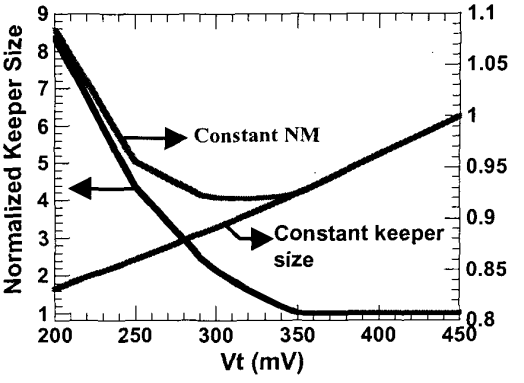


**Figure 4: The normalized delay and keeper size vs. Vt.**

## III. CONTENTION-FREE DOMINO

As it was shown in the previous section, the contention between the keeper's current and the NMOS devices' in the evaluation phase represents a trade-off between NM and speed as Vt decreases. To resolve this trade-off and remove the contention, the new modified Domino gate, CF-Domino, shown in figure 5, was devised.

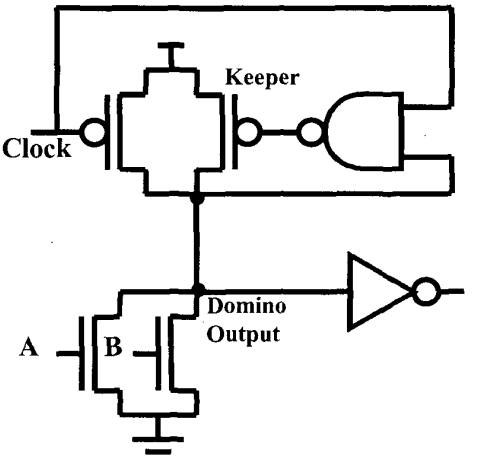


**Figure 5: A 2-input CF-Domino NOR gate.**

The inverter in the conventional Domino that drove the keeper was replaced by a 2-input CMOS NAND gate with one input connected to the Domino output and the other connected to the clock. The devices in the NAND gate that are connected to the clock input are kept at a minimum size to avoid increasing the clock load.

***Circuit Operation:*** The circuit operates as follows; during pre-charging when the clock is low, the NAND's output is high and hence the keeper is **OFF**. Now when the clock goes high if the Domino output remains high, the NAND's output will go low after one gate delay (hence turning the keeper **ON**). However, if the Domino output starts going low, the NAND's output will remain high, and the keeper will remain **OFF**. This totally eliminates the contention between the keeper and the NMOS devices in the evaluation phase since they wont be **ON** simultaneously. Hence, the keeper's size can be increased as Vt is lowered to keep the NM constant without worrying about increasing the contention.

This contention-free operation is clearly demonstrated in Figure 6, which shows the voltage waveforms of the CF-Domino gate in the evaluation phase. It shows how the NAND's output (the keeper input) remains high when the output goes low in the evaluation phase. The small 'dip' in the NAND's output is far from sufficient to start turning the keeper **ON**. Also, it is worth noting that the CF-Domino gate does not require any special clock timing different from that of the conventional Domino as evident from Figures 2 and 6.

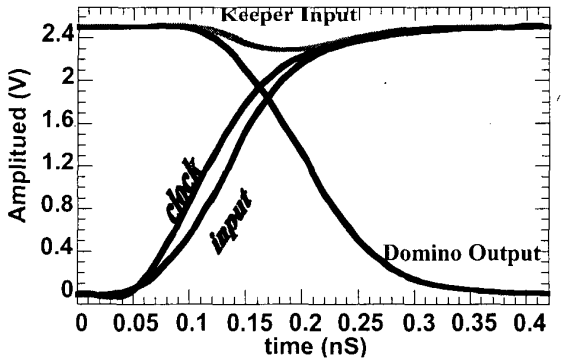


**Figure 6: Voltage waveforms of the CF-Domino gate.**

***Speed Comparison:*** The delay of a 3-stages 8-input CF-Domino NOR chain (**$Fan_{Out}$** = 3) is shown in Figure 7 versus Vt. Also, the delay curves of conventional Domino with constant NM and constant keeper size (from Figure 4) are re-plotted on the same graph. All delays are normalized to the delay of conventional Domino at the high Vt of 450 mV. This figure shows how the speed of the CF-Domino continues to improve as Vt is reduced in a similar manner to that of Domino with constant keeper size. Hence, the speed-NM trade-off has been completely resolved with the CF-Domino. A small speed difference starts to develop between the CF-Domino and conventional Domino with constant keeper size as Vt is reduced. This is due to the increased loading at the output as the keeper and NAND gate are sized up to keep the NM constant.

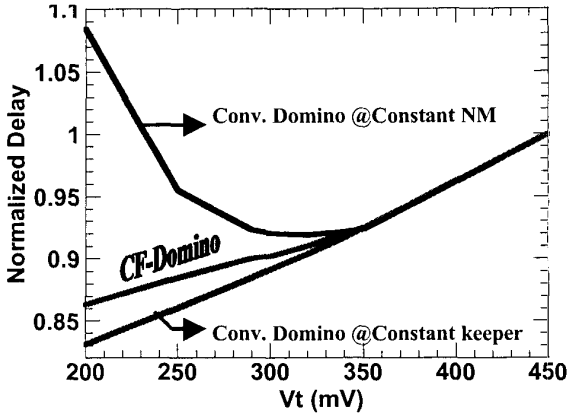


**Figure 7: The normalized delay of CF-Domino vs. Vt. Also shown are the two cases of conventional Domino; constant NM & constant keeper size.**

***Dynamic Power Comparison:*** One potential concern about the new CF-Domino circuit was its dynamic power consumption relative to that of the conventional Domino. This is because of its slightly higher clock loading. Figure 8 shows a dynamic power comparison between the two circuits at 500 MHz. The NOR chains that were used to measure the delays were also used to measure the dynamic power. The dynamic powers, which include the power in the clock circuitry, were normalized to the power of the CF-Domino at high Vt. This Figure shows that the CF-Domino actually has significantly smaller power consumption than the conventional Domino at lower Vts. This is due to the lack of contention in the CF-Domino gate, which means that there are no rush-through currents between VDD and GND during switching.

***Leakage Comparison:*** Figure 9 shows the leakage of the conventional Domino versus Vt normalized to its value at high Vt. It also shows the ratio between the CF-Domino leakage to that of the conventional Domino. The leakage of

the conventional Domino follows a typical exponential curve as Vt is decreased and the ratio remains in the range between 93% to 95%. Hence, the CF-Domino actually has a slightly smaller leakage than the conventional Domino. The smaller leakage is due to the use of the NAND gate instead of an inverter. The series connected NMOS devices will have less leakage due to the de-biasing of the internal node (which makes $V_{GS}$ negative for the top NMOS).

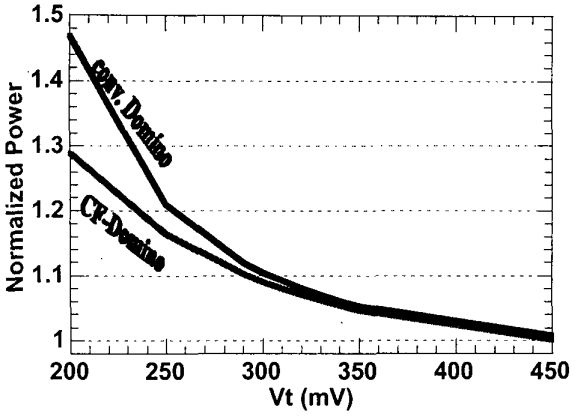


**Figure 8: The normalized dynamic powers of CF-Domino and conventional Domino vs. Vt at 500 MHz. Both circuits had equal and constant NM.**

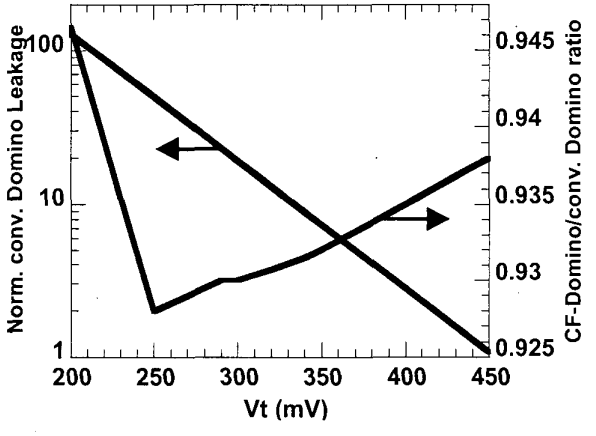


**Figure 9: The normalized leakage of the conventional Domino and leakage ratio between the CF-Domino and conventional Domino.**

***Area Impact:*** The area impact of using the CF-Domino instead of the conventional Domino for the NOR chains used above was less than 3%. This is because the NAND gate that replaced the inverter is of minimum size, hence the insignificant increase in the area.

## IV. CONCLUSION

A new contention-free Domino logic is developed. It resolves the trade-off between noise margins and speed that exists in the conventional Domino circuits. This trade-off prevented the conventional Domino from benefiting from the scaling down of the technologies and supply voltages since it could not tolerate the lower threshold voltages. This in turn meant that expensive dual Vt technologies had to be used if Domino is to continue to be used in future scaled technologies. The speed of the CF-Domino continues to improve as the threshold voltages are scaled down while its noise margins are kept constant. This enables the usage of single low Vt devices in scaled down technologies while retaining the speed advantage of Domino. It was also shown that the CF-Domino consumes less dynamic power than the conventional Domino due to its contention-free operation. It also has less leakage and does not impact the total area significantly.

## V. REFERENCES


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