PAPER

A Contention-Free DOMINO Logic for Scaled-Down CMOS

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SUMMARY A new contention-free Domino logic (**CF-Domino**) that is especially suited for low threshold voltage (**LVT**) is reported. Its superior noise margin and speed over conventional Domino circuits for LVTs are demonstrated using **HSPICE**® simulations and a 0.25 μm CMOS technology with a supply voltage of 2.5 V. The impacts of the new technique on dynamic and leakage powers and area were evaluated. At a 3% area increase, and keeping the noise margins constant, the new **CF-DOMINO** achieves 20% less delay than conventional DOMINO as the threshold voltage scales from 450 mV down to 200 mV. It also achieved 13% less dynamic power and 5% less leakage at that threshold voltage.

key words: *DOMINO logic, digital CMOS circuits, voltage and threshold scaling*

1. Introduction

Since the emergence of dynamic CMOS (DOMINO) gates [1], shown in Fig. 1, they became the main option for implementing high-speed logic paths. Their speed and area advantage over static CMOS circuits [2] makes them indispensable for high performance applications such as microprocessors. However, as the chips' power grew up, lowering the supply voltage has emerged as the most favorable way of reducing the power [3]. To prevent speed degradation, threshold voltages had to be lowered as well, which in turn increased the leakage currents. While the increased leakage does not affect the functionality of static CMOS, it reduces the noise margins (**NM**) of dynamic circuits and ultimately causes their failure. Dual $\mathbf{V_t}$ (**DVT**) technologies were proposed as a solution to this problem [4], where **LVT** devices are used in static CMOS gates and high $\mathbf{V_t}$ (**HVT**) devices are used in Domino gates. This option not only is more expensive than the single $\mathbf{V_t}$ option, but it also deprives the Domino gates from benefiting from the higher speed of the **LVT** devices, thus reducing the Domino's speed advantage. Also, as it was clearly demonstrated in [4], for the same channel length, it is not possible to optimize two devices with two different $\mathbf{V_t}$s. This means that the **HVT** device would have a more compromised performance than a similar device in a single $\mathbf{V_t}$ technology, further degrading the Domino's performance. All this makes it very difficult for products to meet their speed targets as the technology and supplies scale down. Another recent dual $\mathbf{V_t}$ implementation of Domino focused on reducing the leakage while reaping the speed advantages of **LVT** devices [5]. However, no attention was paid to noise margins. This is very impractical since Domino is especially vulnerable to noise. In this work, a modified Domino gate that is contention-free (**CF-Domino**) is proposed to resolve the trade-off between speed and NM and extend the Domino's operation into the deep **LVT** regime. The trade-off between **NM** and speed for the conventional Domino is first demonstrated as a function of $\mathbf{V_t}$ and then the performance of the **CF-Domino** circuit is presented.

2. Conventional DOMINO

Referring to Fig. 1, the conventional Domino operates as follows. During the pre-charge phase (when the clock is low), the Domino output is pre-charged to VDD and the keeper is turned **ON**. When the clock goes high (the evaluation phase), depending on the inputs, the Domino output is either discharged to GND or remains high at VDD. If all inputs are low, the keeper will keep the output high despite any existing noise. So the larger the keeper width ($\mathbf{W_{keeper}}$), the better the **NM**. When at least one of the inputs is high, the output is pulled low and the keeper is turned **OFF**. The

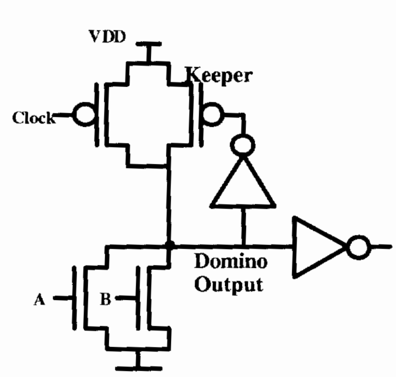

Fig. 1 A 2-input conventional Domino **NOR** gate.

Manuscript received July 9, 2001.
Manuscript revised November 5, 2001.

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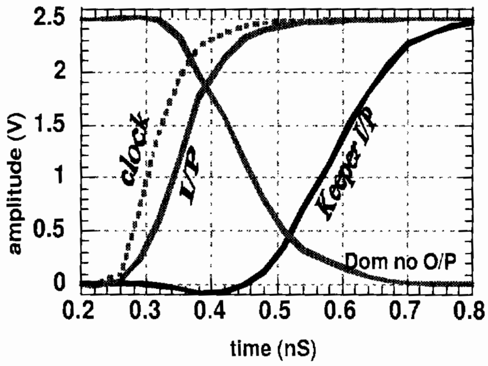

Fig. 2 The waveforms of a conventional Domino gate.

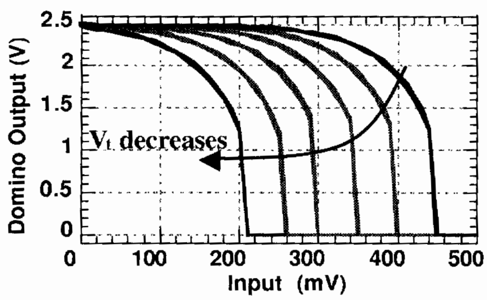

Fig. 3 The DC characteristics of Domino as a function of $\mathbf{V_t}$.

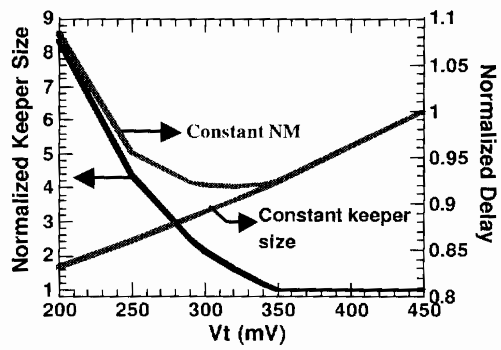

Fig. 4 The normalized delay and keeper size versus $\mathbf{V_t}$.

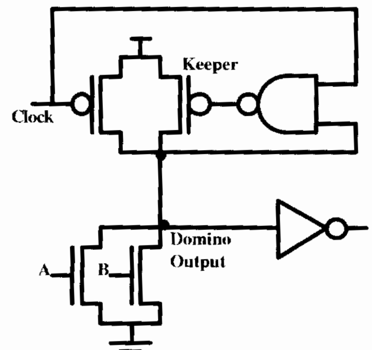

Fig. 5 A 2-input **CF-Domino NOR** gate.

larger the keeper, the larger the contention that occurs between the pulling down NMOS device and the keeper and the slower the gate. This is the basic speed-**NM** trade-off of the conventional Domino. This trade-off becomes severer at lower $\mathbf{V_t}$s because of the increased NMOS leakage. Figure 2 shows the voltage waveforms of a Domino gate. It shows how the Domino output starts switching while the keeper is still **ON** (the contention). Figure 3 shows the DC characteristics of an 8-input conventional Domino **NOR** gate for several $\mathbf{V_t}$s keeping the keeper size constant and tying all inputs together. An 8-input **NOR** was chosen because Domino is mostly favoured for wide $\mathbf{Fan_{In}}$ NOR gates and these represent the worst-case scenario for leakage-induced noise margins degradation. This figure shows that the low **NM** decreases as $\mathbf{V_t}$ decreases. Figure 4 shows the normalized delay of a 3-stages chain of 8-input Domino **NOR** gates with a $\mathbf{Fan_{Out}}$ of 3 versus $\mathbf{V_t}$ for two cases; constant **NM** (by varying the keeper's size) and constant keeper size (i.e. variable **NM**). The normalized keeper size for the constant **NM** case is also shown on the same graph. The **NM** was defined according to the criterion in [4], the input voltage above ground that causes a 10% drop from VDD at the Domino output. The **NM** was set to 10% of VDD. This figure shows the trade-off between **NM** and speed as $\mathbf{V_t}$ is reduced. In order to keep the **NM** of the Domino gate constant, the keeper size had to be increased. This, in turn reduced the speed gain at lower $\mathbf{V_t}$s and eventually increased the delay. The constant keeper curve shows the maximum possible gain in speed with lowering the $\mathbf{V_t}$. However, in the case of conventional Domino, this can only be achieved if the reduction in the **NM** with $\mathbf{V_t}$ was wrongfully ignored.

3. Contention-Free DOMINO

3.1 Circuit Description

As it was shown in the previous section, the contention between the keeper's current and the NMOS devices' in the evaluation phase represents a trade-off between **NM** and speed as $\mathbf{V_t}$ decreases. To resolve this trade-off and remove the contention, the new modified Domino gate, **CF-Domino**, shown in Fig. 5, was devised. The inverter in the conventional Domino, that drove the keeper, was replaced by a 2-input static CMOS **NAND** gate. One input of the **NAND** gate is connected to the Domino output and the other is connected to the clock. The devices in the **NAND** gate that are connected to the clock input are kept at a minimum size to avoid increasing the clock load. This technique is only valid for footless Domino, where all inputs are synchronized with the clock. A conditional keeper technique similar to the **CF-Domino** was proposed in [6], [7]. In that technique, the **NAND** clock input is delayed (by at least 2 inverters). This means that the DOMINO output would actually be without a keeper for this delay, a potential serious noise problem for the already noise sensitive Domino. Also, for this technique to be efficient in reducing the gate's delay, the fan in has to be very high (>16) [6]. The added inverters also increase the power consumption. In the presented **CF-Domino** technique, if there is a need to delay the clock (to mach the data delays), the gate won't suffer the above shortcomings.

3.2 Circuit Operation

The circuit operates as follows; during pre-charging when the clock is low, the **NAND**'s output is high and hence the keeper is OFF. Now when the clock goes high if the Domino output remains high, the **NAND**'s output will go low after one gate delay and turns the keeper ON. However, if the Domino output starts going low, the **NAND**'s output will remain high, and the keeper will remain OFF. This totally eliminates the contention between the keeper and the NMOS devices in the evaluation phase since they will not be ON simultaneously. Hence, the noise margin is kept constant (and equal to its value at high $\mathbf{V_t}$) as $\mathbf{V_t}$ is lowered by increasing the keeper's size. At the same time (as the keeper's size increases) the contention does not increase. In fact, the noise margin of the **CF-Domino** circuit can be made identical to that static CMOS. This contention-free operation is clearly demonstrated in Fig. 6, which shows the voltage waveforms of the **CF-Domino** gate in the evaluation phase. It shows how the **NAND**'s output (the keeper input) remains high when the output goes low in the evaluation phase. The small 'dip' in the **NAND**'s output is far from sufficient to start turning the keeper ON. Also, it is worth noting that the **CF-Domino** gate does not require any special clock timing different from that of practical conventional Domino as evident from Figs. 2 and 6. Just as in regular Domino, the clock is usually delayed such that precharging is delayed along the logic path to increase the operating frequency [8]. The clock, however, is never delayed to the point that it gets into the path delay (i.e. clock is never designed to arrive after the data). This is usually accomplished by using two inverters to delay the clock between consecutive Domino stages (which have a static CMOS stage in between). If the delay between the clock and data becomes too large, the **CF-Domino** operation will resemble that of the conventional Domino (i.e. it will suffer from contention). Finally, if the Domino path contains feed forwarded data (i.e. some inputs to a Domino gate arriving earlier than the others), fast inputs should be delayed to avoid the above pitfall.

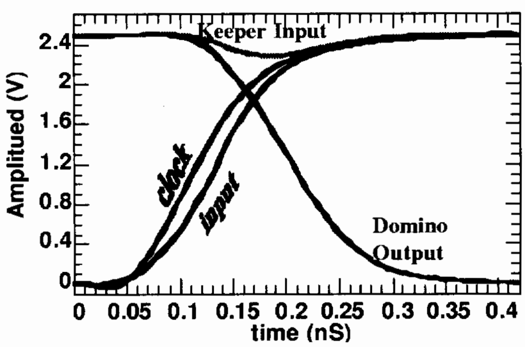

Fig. 6 Voltage waveforms of the **CF-Domino** gate.

3.3 Speed Comparison

The delay of a 3-stages 8-input **CF-Domino NOR** chain with a fanOut of 3 is shown in Fig. 7 as a function of $\mathbf{V_t}$ for constant **NM**. Also, the delay curves of conventional Domino (same setup, Fan in and Fan out) with constant **NM** and constant keeper size (from Fig. 4) are re-plotted on the same graph. All delays are normalized to the delay of the conventional Domino at the high $\mathbf{V_t}$ of 450 mV. This figure shows how the speed of the **CF-Domino** continues to improve as $\mathbf{V_t}$ is reduced in a similar manner to that of Domino with constant keeper size. Hence, the speed-**NM** trade-off has been completely resolved with the **CF-Domino**. A small speed difference starts to develop between the **CF-Domino** and conventional Domino with constant keeper size as $\mathbf{V_t}$ is reduced further. This is due to the increased loading at the output as the keeper and **NAND** gate are sized up to keep the **NM** constant.

3.4 Dynamic Power Comparison

A potential concern about the **CF-Domino** circuit is its dynamic power consumption relative to the conventional Domino. This is because of its slightly higher clock loading. Figure 8 shows a dynamic power comparison between the two circuits at 500 MHz. The **NOR** chains that were used to measure the delays were also used to measure the dynamic power. The dynamic powers, which include the power in the clock circuitry, were normalized to the power of the **CF-Domino** at high $\mathbf{V_t}$. This figure shows that the **CF-Domino** actu-

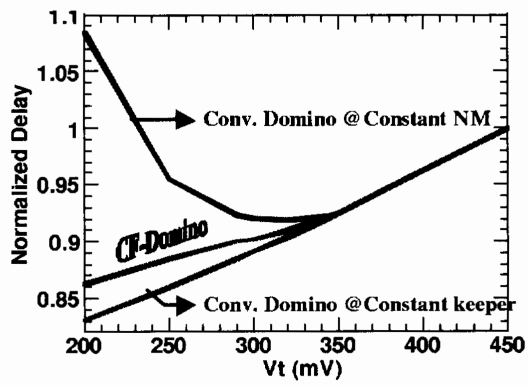

Fig. 7 The normalized delay of the **CF-Domino** versus $\mathbf{V_t}$. Also shown are the two cases of conventional Domino; constant **NM** & constant keeper size.

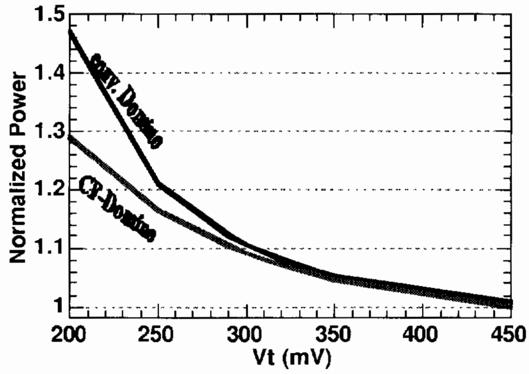

Fig. 8 The normalized dynamic powers of **CF-Domino** and conventional Domino versus $\mathbf{V_t}$ at 500 MHz. Both circuits had equal and constant **NM**.

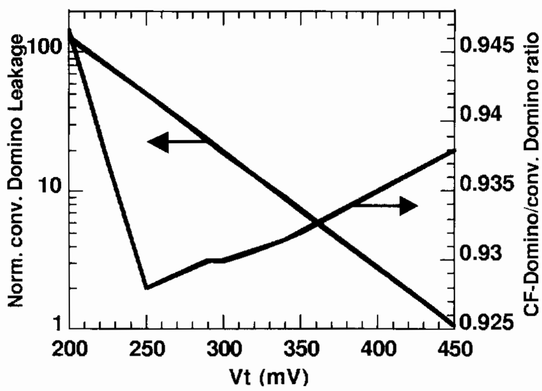

Fig. 9 The normalized leakage of conventional Domino and leakage ratio between **CF-Domino** and conventional Domino.

ally has significantly smaller power consumption than the conventional Domino at lower $\mathbf{V_t}$s. This is due to the lack of contention in the **CF-Domino** gate, which means that there are no rush-through currents between VDD and GND during switching.

3.5 Leakage Comparison

Figure 9 shows the leakage of the conventional Domino versus $\mathbf{V_t}$ normalized to its value at high $\mathbf{V_t}$. It also shows the ratio between the **CF-Domino** leakage to that of the conventional Domino. The leakage of the conventional Domino follows a typical exponential curve as $\mathbf{V_t}$ is decreased and the ratio remains in the range between 93% to 95%. Hence, the **CF-Domino** actually has a slightly smaller leakage than the conventional Domino. The smaller leakage is due to the use of the **NAND** gate instead of an inverter. The series connected NMOS devices will have less leakage due to the de-biasing of the internal node (which makes $\mathbf{V_{GS}}$ negative for the top NMOS).

3.6 Area Impact

The area impact of using the **CF-Domino** instead of the conventional Domino for the **NOR** chains used above was less than 3%. This is because the **NAND** gate that replaced the inverter is of minimum size, hence the insignificant increase in the area.

4. Conclusions

A new contention-free Domino logic is developed. It resolves the trade-off between noise margins and speed that exists in the conventional Domino circuits. This trade-off prevented the conventional Domino from benefiting from the scaling down of the technologies and supply voltages since it could not tolerate the lower threshold voltages. This in turn meant that expensive dual $\mathbf{V_t}$ technologies had to be used if Domino is to continue to be used in future scaled technologies. The speed of the **CF-Domino** continues to improve as the threshold voltages are scaled down while its noise margins are kept constant. This enables the usage of single low $\mathbf{V_t}$ devices in scaled down technologies while retaining the speed advantage of Domino. It was also shown that the **CF-Domino** consumes less dynamic power than the conventional Domino due to its contention-free operation. It also has less leakage and does not impact the total area significantly.

Acknowledgement

The authors are grateful for the facilities support provided by KFUPM. This work is supported in part by NSERC and Micronet of CANADA.

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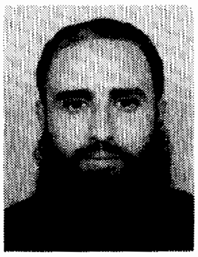

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