A Portable Clock Recovery Circuit (CRC) For Systems-On-Chip Serial Data Communication

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Abstract— **An all-digital clock recovery circuit that is capable of extracting the clock embedded in the serial data stream is presented. The new CRC can retime the output clock with the received data within two bit transitions. The absence of analog filters or other analog blocks gives it a much smaller area than conventional circuitry. Also, being fully-digital, it can be described, simulated and synthesized using hardware description languages and be ported to any technology (thus supporting system on a chip designs). Circuit operation and performance was demonstrated using a 0.13µm, 1.2V CMOS technology and T-Spice® simulations.**

I. Introduction

High achievable data rates and reliability have made serial communications the most preferred inter-chip communication method. Applications range from backplane communications, to fiber data transmission. Also, as the on-chip global interconnect technology moves from ad-hoc wiring or bus-based to switch/router based schemes [1], the demand for low overhead, low-power and portable serial communication circuits (as IP blocks for link implementation) will be ever increasing.

A crucial part of non return-to-zero (NRZ) serial communication is the clock recovery and data retiming circuitry. These circuits, setting in the repeaters and receivers, accurately extract the clock signals from non return-to-zero (NRZ) serial bit streams where they are embedded. They must maintain synchronism between the generated clock and the data in the presence of data phase noise (jitter), supply and temperature fluctuations. Also, they must be agile in extracting synchronized clocks for different data packets arriving from different sources.

The job of clock recover circuits is further made difficult due to the nature of random NRZ data; they have no spectral contents at the bit rate or its even-order harmonics [2, 3]. This problem can be circumvented using edge detection techniques. Also, long streams of consecutive 1s and 0s represent a serious problem to traditional clock recovery circuits that utilize Phase-Locked-Loops (PLLs) and result in data-dependent jitter in the PLL's output. To reduce this jitter the PLL's bandwidth has to be limited which in turn limits the PLL's capture range. Also, larger loop gain reduces jitter generation but reduces stability.

Analog PLLs suffer from several shortcomings; large area (due to analog blocks), difficulty to port to other processes or supplies, high VCO operating frequency (double the data frequency) which in turn limits the data rate, phase error accumulation in the VCO, and long lock times due to the loop damping behavior.

Fully digital or semi-digital solutions were proposed to solve some of the analog PLLs problems [4-7]. Though these techniques retain many of the analog features, they suffer from poor resolution (more jitter), stability issues (two or more loops interacting), difficulty to port from one process to another (due to analog blocks) and/or large areas. A fully digital non PLL/DLL technique for source synchronous serial communication (clock frequency available, but the phase needs re-timing) demonstrated the potential of digital circuits in clock recovery and data re-timing [8]. In this work a novel non PLL/DLL digital technique for clock recovery and re-timing is introduced. The clock frequency is captured from the NRZ data stream and is aligned with the data. The circuit retimes the clock with each data transition.

The basic operation and circuit description of the proposed clock-recovery circuit (**CRC**) are given in section 2. Performance evaluations are presented in section 3 followed by conclusions in section 4.

II. The Proposed CRC

A. Basic Concept of Operation

The basic idea of the CRC is to use a variable length digital delay line to measure the input data's bit duration (i.e. the time between a positive edge and a negative edge). This delay is then used in a feedback loop to form an oscillator with an oscillation period equal to that delay (i.e. oscillation frequency will be twice the maximum data rate).

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The architecture of the proposed CRC is shown in Figure 1. When the incoming NRZ data (**Din**) exhibits a positive transition (0→1), the positive-edge detector (**PED**) circuit produces a pulse ($\mathbf{P_0}$) that would travel down a delay line. The delay line will provide several phases of this pulse ($\mathbf{P_1}$ to $\mathbf{P_n}$). An identical delay line will also contain a replica of this pulse, providing unloaded clock phases ($\mathbf{CLK_0}$ to $\mathbf{CLK_n}$). When the next negative NRZ data edge arrives, the negative-edge detector (**NED**) circuit will generate two complementary pulses, **T** and $\mathbf{T_b}$, which will be used to latch in the appropriate pulse phase. This latched pulse phase is then used as an enable signal for a mux to select the corresponding clock phase. More than one clock phase might be selected, making the resulting feedback clock ($\mathbf{Clk_{fb}}$) an interpolated version of the selected clock phases, enhancing the CRC's resolution significantly. This feedback clock is then re-constructed using a simple Schmitt Trigger before it is fed back to the **PED** circuit. This closes the loop and forms a ring oscillator with a total delay of 1 bit duration (i.e. bit cell).

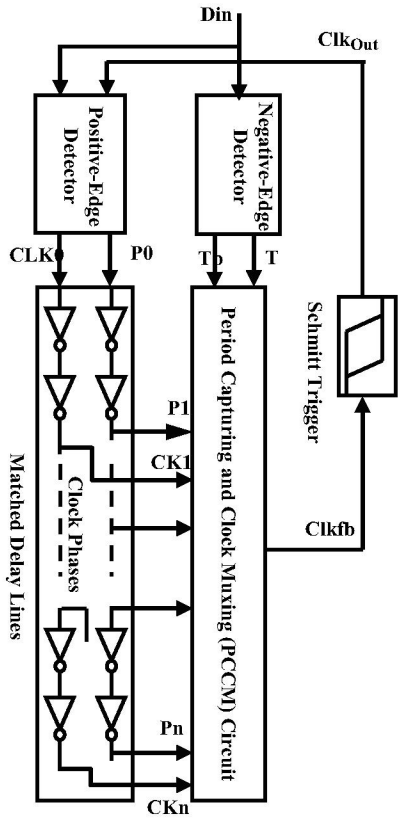


Figure 1. The architecture of the proposed clock-recovery circuit.

The CRC will oscillate at twice the input's frequency and from this point onward it will continue to oscillate even with the absence of any positive or negative input data edges. With each data transition the circuit re-times the clock with data, hence correct for any injected phase and/or frequency noise.

B. Circuit Description

The proposed CRC circuit has five main components; a positive-edge detector circuit (**PED**), a negative-edge detector circuit (**NED**), two delay lines, a period capturing and clock muxing (**PCCM**) circuit, and a Schmitt Trigger. All blocks are implemented using standard CMOS circuits.

Figure 2 shows the schematics of the PED and NED circuits. The **PED** circuit (Figure 2 (a)) generates narrow output pulses for every positive transition in the NRZ input data or feedback clock. The output pulses have a width of 3 inverter's delay. Adding more inverters in the second input path of the NAND gates can increase the width of the output pulses. These pulses are used to re-synchronize the output clock of the CRC with the input data (in the absence of data transitions the output clock will remain at the same frequency and phase). An odd number of inverters are used to delay these pulses by a fixed delay. The amount of required delay depends on the intended range of data frequencies.

The **NED** circuit is similar to the PED except that it generates 2 complementary output pulses (T and Tb) only when the input data exhibits a negative transition. These pulses are used by the PCCM circuit to latch the appropriate phase(s) of the clock pulse (from CK0 to CKn). The matching delay matches the delay of PCCM and Schmitt trigger circuits.

Figure 3 shows the circuit diagram of the period capturing and clock muxing circuit along with the simple Schmitt trigger used. The basic block is a pulsed flip-flop (PFF) whose inputs come from one of the identical delay lines and are triggered by the complementary pulses T and Tb. The output of each PFF controls a transmission gate. When a clock pulse coincides with T and Tb, the PFF will latch a 1 and hence turn on the corresponding transmission gate which will connect the selected clock phase (from the second delay line) to the output. The delay lines are made of simple CMOS inverters.

The total number of gates in the CRC is less than 100, most of which are inverters. This makes the circuit very compact allowing the instantiation of many copies for different serial links within the same chip.

III. PERFORMANCE EVALUATION

Circuit simulations using T-Spice® and a 0.13μm, 1.2V CMOS technology were used to evaluate the operation and performance of the proposed circuit. Sizes of transistors in the circuit components were optimized for 2 GBPS operation, but it can still operate with any input frequency up

to 2.5 GBPS. For lower frequencies the fixed delay in the PED circuit is increased keeping the ELCM circuit the same.

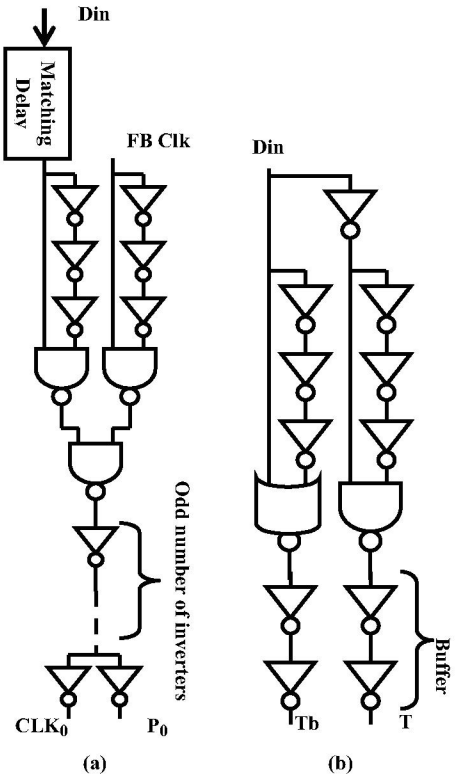


Figure 2. (a) The positive-edge detector circuit, (b) The negative-edge detector.

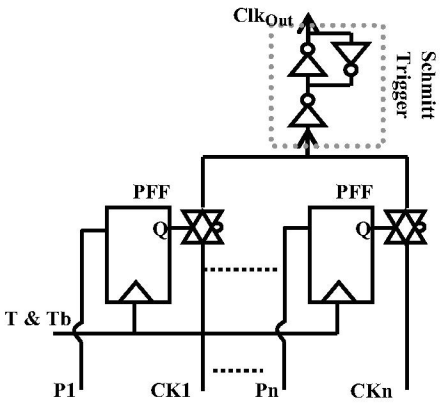


Figure 3. The PCCM Circuit's Schematic including the Schmitt Trigger.

A. Basic Operation

Figure 4 below shows how the CRC captures the data frequency at 2 GBPS and generates an output clock after two bit transitions. The data pattern used was 1011111111.

Figure 5 shows how the circuit fully recovers the clock within two data transitions after a large phase noise (equivalent to a half bit cell) is injected into the input data. An analog PLL would have taken hundreds or even thousands of cycles to recover.

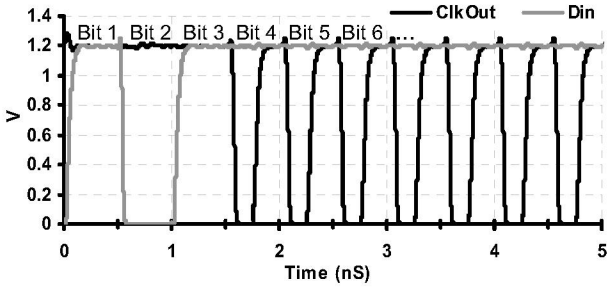


Figure 4. The output clock waveform at 2 GBPS.

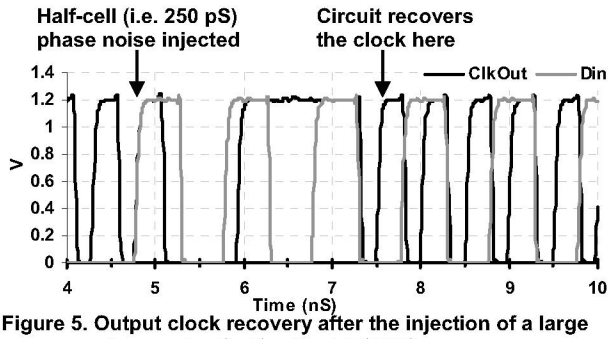


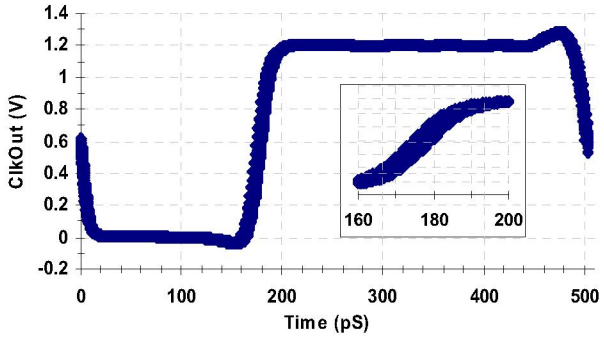
Figure 5. Output clock recovery after the injection of a large phase noise (half-cell) at 2 GBPS.

B. Stability of Output Frequency

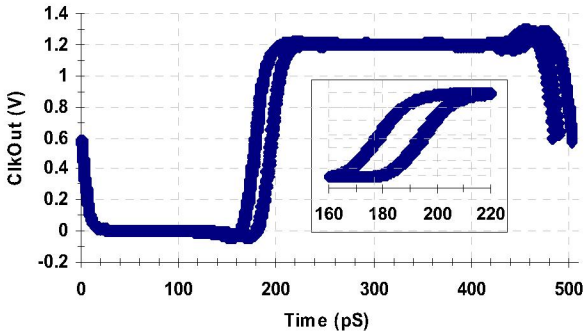
A major concern of using a digital circuit in clock recovery might arise; that is the stability of the output frequency. To evaluate the stability of the output clock's frequency, two simulations were carried out; one with no data transitions after the initial clock frequency capturing (i.e. data stays constant after the two initial bit transitions) and another with a pseudo-random input stream (using 6-bit long pseudo-random patterns that are fed serially to the circuit). The output clock periods were laid out on top of one another in Figure 6 (a) and (b).

As this figure shows, the peak-to-peak period jitter in the case of no data transitions is less than 10 pS. This is an outstanding performance for an all-digital clock recovery circuitry. The results in Figure 6(b) show that the output clock has two modes with about 10 pS difference in their periods. The peak-to-peak period jitter within each mode is still less than 10 pS. These two modes result from variations in the loop delay due to two modes of operation; when there is no positive data transition and when there is such transition. As Figure 2(a) shows, the delay of the PED circuit is slightly smaller when there is a positive input data transition (since in this case both inputs to the second NAND gate are going high). This bi-modal operation of the CRC won't cause bit errors since the faster mode only occur when there is an input transition and the circuit immediately goes back to the normal mode when there is no data transitions

(i.e. there is no accumulation of phase error). It should be noted that the relative difference between the two modes will be smaller for lower clock frequencies.



(a) Output Clock with no data transitions after the first two



(b) Output Clock with pseudo-random data

Figure 6. Output Clocks laid on top of one another. The insets show a Zoom-in of clock edge region.

Figure 7 shows the average output clock period for different data rates. The circuit components were only optimized once for the 2 GBPS data rate (0.5 nS bit cell). For other data rates, only the fixed delay part of the PED circuit was changed (by changing the number of inverters at its output). As the results in the figure indicate, the maximum frequency error is still below 0.8% for other data rates. The accumulated phase error due to the frequency error, however, is reset with every time a data transition occurs. This means that with proper data encoding that ensure adequate data transitions, the bit error rate can be set to a desired value.

IV. CONCLUSIONS

An all-digital clock-recovery circuit has been developed. The proposed circuit can capture the clock frequency of an NRZ data stream within two bit transitions. Simulation results show that the output clock frequency of the circuit is very stable. Output frequency error could be made very small by proper sizing of the circuit components for the intended technology. However, the circuit continuously re-times the clock phase with each bit transition. This means that with adequate data encoding the impact of frequency error on bit error rate can be virtually eliminated. The circuit has less than 100 gates (most of which are inverters). This makes it very compact, highly portable and can support SoC designs with many serial links for inter-chip or intra-chip communications..

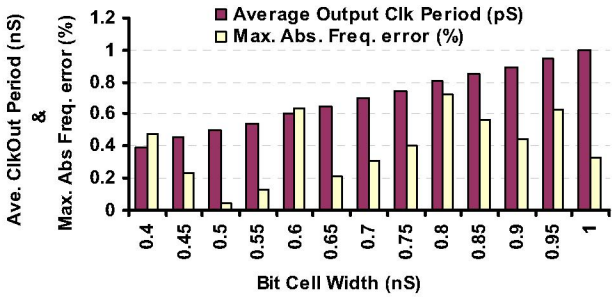


Figure 7. The average output clock Frequency and maximum absolute frequency error for different data rates.

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