King Fahd University of Petroleum & Minerals
Computer Engineering Dept

EE 202 – Digital Logic Circuit Design

Term 151

Dr. Ashraf S. Hasan Mahmoud

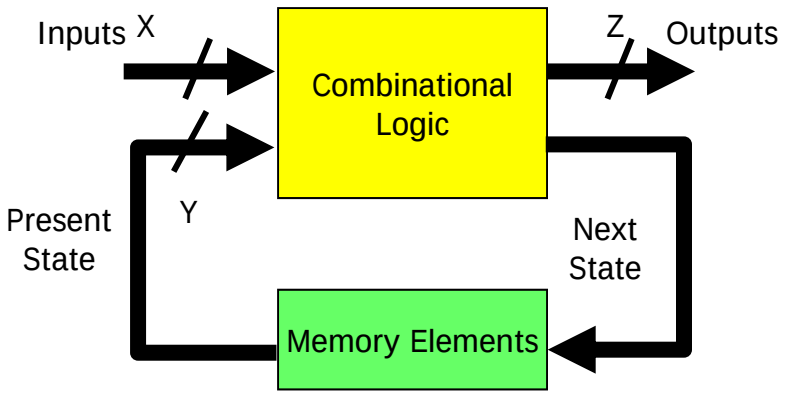
Rm 22-420

Ext. 1724

Email: ashraf@kfupm.edu.sa

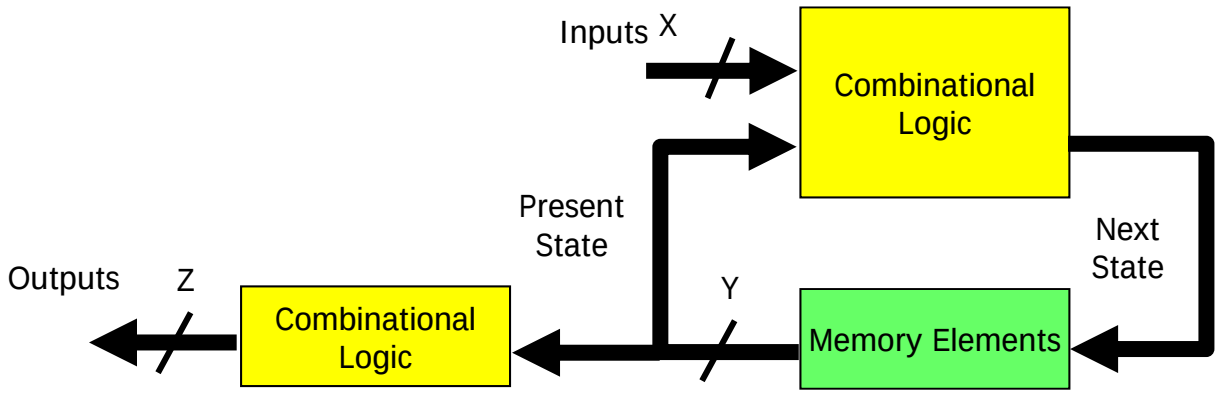
Mealy and Moore Type Finite State Machines

- Mealy Machine:
  - In a Mealy machine, the outputs are a function of the present state and the value of the inputs as shown in figure.
  - The outputs may change asynchronously in response to any change in the inputs.



Mealy and Moore Type Finite State Machines – cont'd

- Moore Machine:
  - In a Moore machine the outputs depend only on the present state as shown in figure.
  - A combinational logic block maps the inputs and the current state into the necessary flip-flop inputs to store the appropriate next state just like Mealy machine.
  - However, the outputs are computed by a combinational logic block whose inputs are only the flip-flops state outputs.
  - The outputs change synchronously with the state transition triggered by the active clock edge



Sequence Recognizer – MOORE Machine Example

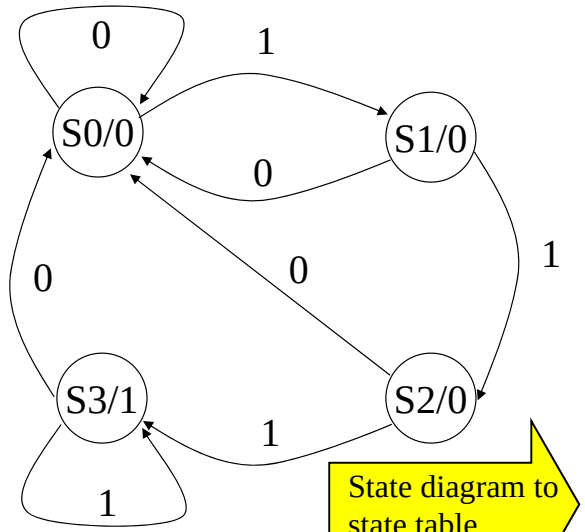
This is the same problem solved in class notes (slide 48 of Unit_4 package)

- Problem: Design a sequence recognizer (state machine) that outputs '1' if the input is '1' for three consecutive clocks – Use MOORE DESIGN – using D flip-flops
- Let input be X; Output be Y
- Solution: State diagram is as shown

  State table is as shown

State assignment (AB):
S0 = 00
S1 = 01
S2 = 10
S3 = 11

Arc label: X
State label: AB/Y



Present State		Input	Next State		Output	*D* Flip-Flops Input	
A	B	X	A	B	Y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1

Sequence Recognizer – MOORE Machine Example – cont'd

Present State		Input	Next State		Output	*D* Flip-Flops Input	
A	B	X	A	B	Y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1

Note that D_A is the SAME as NEXT STATE A (or A^+ or A(t+1)) – same applies to D_B.

State table to Equations for F/F inputs and output

A \ BX	00	01	11	10
0	0	0	1	0
1	0	1	1	0

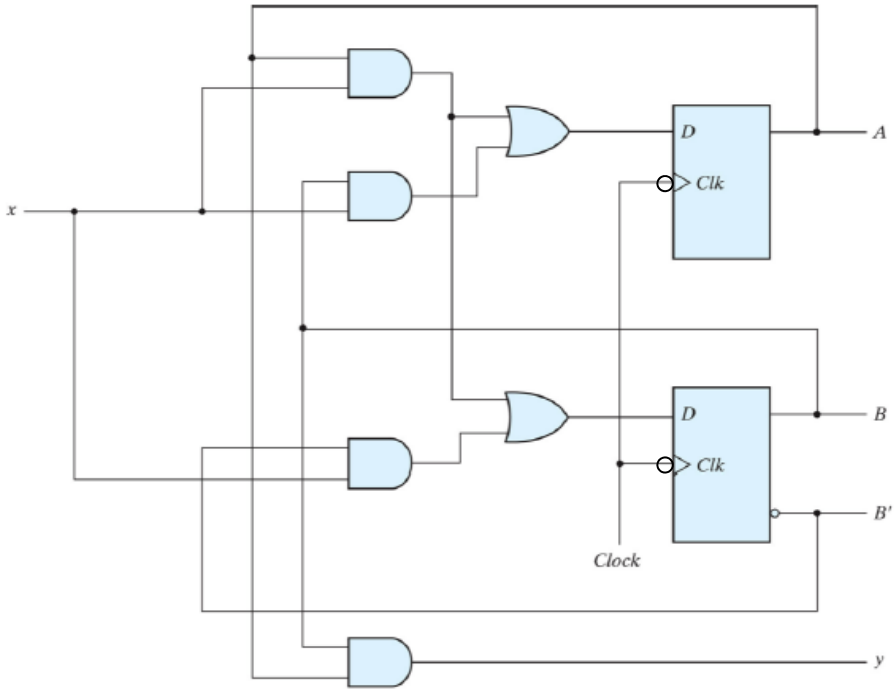
$D_A = AX + BX$

A \ BX	00	01	11	10
0	0	1	0	0
1	0	1	1	0

$D_B = AX + B'X$

A \ BX	00	01	11	10
0	0	0	0	0
1	0	0	1	1

$Y = AB$



Notice we chose to use D F/F that respond on –ve clock edge

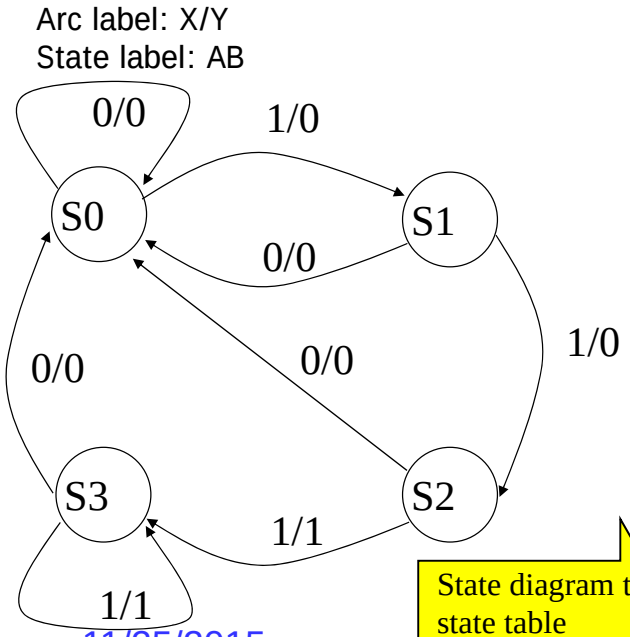
Equations to actual circuit

Sequence Recognizer – MEALY Machine Example

- Problem: Design a sequence recognizer (state machine) that outputs '1' if the input is '1' for three consecutive clocks – Use MEALY DESIGN – using D flip-flops
- Let input be X; Output be Y
- Solution: State diagram is as shown

  State table is as shown

State assignment (AB):
S0 = 00
S1 = 01
S2 = 10
S3 = 11



State diagram to state table

Present State		Input	Next State		Output	*D* Flip-Flops Input	
A	B	X	A	B	Y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	**1**	1	0
1	1	0	0	0	**0**	0	0
1	1	1	1	1	1	1	1

Sequence Recognizer – MEALY Machine Example – cont'd

Present State		Input	Next State		Output	*D* Flip-Flops Input	
A	B	X	A	B	Y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	**1**	1	1
1	1	0	0	0	**0**	0	0
1	1	1	1	1	1	1	1

Note DA and DB are same as before – Y variable is different

State table to Equations for F/F inputs and output

A \ BX	00	01	11	10
0	0	0	1	0
1	0	1	1	0

$D_A = AX + BX$

A \ BX	00	01	11	10
0	0	1	0	0
1	0	1	1	0

$D_B = AX + B'X$

A \ BX	00	01	11	10
0	0	0	0	0
1	0	1	1	0

$Y = AX$

Equations to actual circuit

Notice we chose to use D F/F that respond on –ve clock edge

You draw the circuit – same as previous circuit but with Y = AX

Sequence Recognizer – MEALY Versus MOORE

- DA and DB – are the same for the two designs since we used the same states and same state assignment scheme (codes)
- The output variable Y is a function of A and X for the Mealy machine while it is a function of A and B for the Moore machine

- We want to see the timing diagram for both circuit and **observe the Y signal**

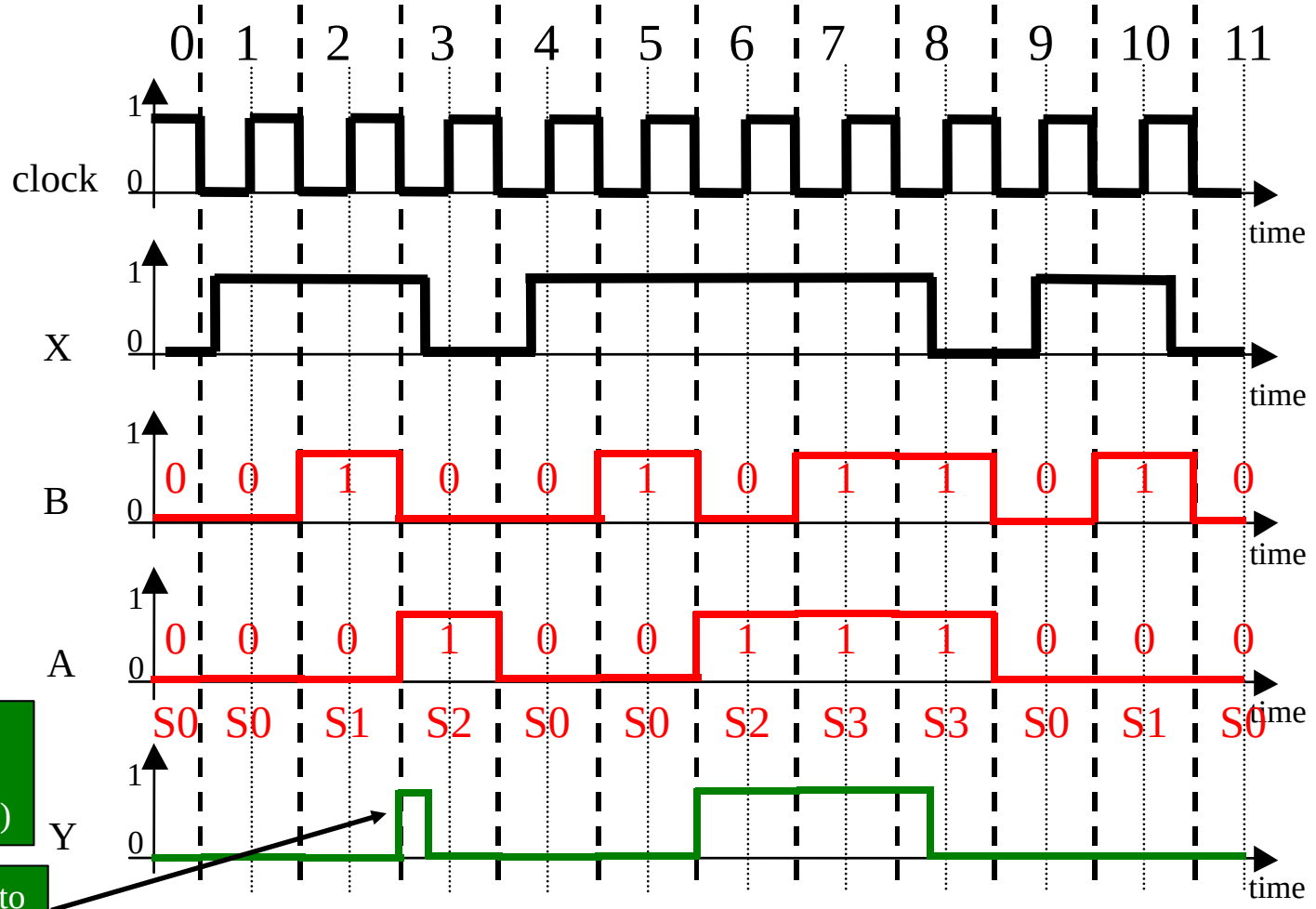
Sequence Recognizer - MEALY Design – Timing Diagram

$D_A = AX + BX$

$D_B = AX + B'X$

$Y = AX$

CLK	10
X	0
A	0
B	1
D_A	0
D_B	0



Note that output Y changes asynchronously (i.e. irrespective of the clock signal)

Note that this may be referred to as false output or a glitch!

Sequence Recognizer - MOORE Design – Timing Diagram

$D_A = AX + BX$

$D_B = AX + B'X$

$Z = AB$

Note that D_A and D_B are the same as before

Note that output Y now is governed by the clock signal Boundaries!