KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 202 Fundamentals of Computer Engineering
Syllabus – Semester 081

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. ***(Prerequisite: PHYS 102)***

Instructor

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Course Material:

1. **Text Book:** Morris Mano and Charles Kime, *Logic and Computer Design Fundamentals*, Third Edition, Prentice Hall International, 2004.

2. **Course CD:** A CD containing all course lectures with animations and sound is available. The material can be downloaded from CCSE network (check with instructor). The material is divided into 6 units with several lessons in each unit. Alternatively, you can ftp it from: ftp://rahma.ccse.kfupm.edu.sa/../../../../export/tools/material/ and pick the "On Line Course Material" folder. Use your CCSE UNIX account credentials for the ftp.

Grading Policy:

Assignments & Quizzes	25%
Exam I	20% (Tues Nov 25th class time)
Exam II	20% (Tues Jan 13th class time)
Final	35%

Attendance Policy

Attendance is required by all students. Official and authorized absence excuse must be presented to the instructor no later than one week following the absence. Unexcused absences lead to a "DEN" grade (university policy).

Course Learning Outcomes Table

Course Learning Outcomes	Outcome Indicators & Details
1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.	➢ Represent integer and fractional values in various number systems ➢ Convert number representation from one system to another ➢ Perform arithmetic operations in various number systems ➢ Represent data in different binary codes including error detecting codes (parity) ➢ Simplify Boolean expressions using Boolean algebra & identities
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.	➢ Derive gate-level implementation of a given Boolean expression and vice versa ➢ Ability to build larger combinational functions using predefined modules (e.g., decoders, multiplexers, adders, Magnitude comparators.)

	➢ Ability to build a state diagram / table for both Moore & Mealy models from functional description ➢ Ability to design & implement Moore & Mealy model synchronous sequential circuits using different Flip-Flop types. ➢ Ability to draw timing diagrams for major signals of both sequential and combination circuits
3. Ability to use CAD tools to simulate and verify logic circuits.	➢ Ability to simulate and verify the operation of combinational circuits ➢ Ability to simulate and verify the operation of sequential circuits

Course Road Map & Weekly Breakdown

Week	Topic	CD Material		Book Ref.
		Unit	Lessons	
1	**Introduction, Number System and Arithmetic**	1	1,2 and 3	1.1-1.3
2	**Number Base conversion and Signed Numbers**	1	4, 5 and 6	5.3-5.4
3	**Signed Numbers Arithmetic and Codes**	1	6	5.4-5.4, 1.4-1.7, plus notes
4	**Binary Logic, Basic Identities, Algebraic Simplification**	1 2	Lesson 7. Lesson 1.	2.1-2.2
5	**Canonical and Standard Forms, Physical Properties of Gates**	2	2 & 3	2.3&3.2
6	**Logic Simplification using K-Maps, K-Maps manipulation**	2	4 & 5	2.4-2.5
7	**2-Level and Multi-level implementations, Universal Gates**	2	6 & 7	2.6-2.8 (3.4)
8	**Combinational Logic Design and MSI Parts**	3	1 & 2	4.3-4.5
9	**MSI Parts and Adders**	3	3 & 4	4.3-4.5, 5.1&5.2
10	**Design with MSI Parts**	3	5, 6, 7	4.6, 5.5-5.6
11	**Sequential Circuits, Latches and FFs**	4	1 & 2	6.1-6.3 & 6.7
12	**Design and Analysis of Sequential Circuits**	4	3 & 4	6.4 -6.6
13	**Analysis of Sequential Circuits**	4	5	6.4-6.6
14	**Registers and Counters**	5	1-4	7.1,7.2, &7.6
15	**PLDs and Memory**	6	1	3.6, 4.6, 9.1, & 9.2(partially)

Online Lessons included on the course CD

	***Unit I* : Number System and Codes**
1	Introduction. Information Processing, and representation. Digital vs Analog quantities.
2	Number Systems. Binary, Octal and Hexadecimal #'s
3	Number System Arithmetic. Binary arith (Addition, Subtraction & Multiplication). Arith in other systems.
4	Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex)
5	Binary Storage & Registers. Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement
6	Signed Binary Addition and Subtraction. R's Complement. Signed Binary Addition and Subtraction. (R-1)'s Complement
7	Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes
	***Unit II* : Binary Logic & Gates**
1	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Algebraic manipulation, Complement of a function.
2	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.
3	Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4	***Map method of simplification***: Two-, Three-, and Four-variable K-Map.
5	***Map manipulation:*** Essential prime implicants, Non-essential prime implicants, Simplification procedure, POS simplification, Don't care conditions and simplification, Five, and Six-variable K-Map.
6	Universal gates; ***NAND, NOR gates:*** 2-level implementation. ***Multilevel Circuits***.
7	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
	***Unit III* : Combinational Logic**
1	Combinational Logic, Design Procedure & Examples.
2	Half and Full Adders, Half and Full Subtractor Ripple Carry Adder design and ***delay*** analysis ***Binary Adders: 4-Bit* Ripple Carry Adder,**
3	**Carry Look-Ahead Adder, Binary Adder-Subtractor**. BCD Adder, Binary Multiplier
4	MSI parts. Decoders, Decoder expansion, combinational logic implementation using decoders, Encoders & Priority Encoders
5	Multiplexers, Function Implementation using multiplexers, Demultiplexers
6	Magnitude Comparator.
7	Examples of MSI designs
	***Unit IV* : Sequential Circuits**
1	***Sequential Circuits:*** Latches, Clocked latches: SR , D, T and JK. Race problem in clocked JK-Latch. ***Function & Excitation Tables of clocked latches:*** SR, D, and JK.
2	***Flip-Flops:*** Master-Slave, T-FF. Function & Excitation Tables of T-FF. ***Asynchronous/Direct Clear and Set Inputs.*** Setup, Hold
3	***Sequential Circuit Design***: Excitation Tables. Design procedure, State diagrams and state tables.
4	***Sequential Circuit Analysis:*** Input equations, State table.
5	Mealy vs. Moore models of FSMs. Examples.
	***Unit V* : Registers & Counters**
1	Registers, Registers with parallel load, Shift Registers. Bi-directional shift register.
2	Synchronous Binary Counters: Up-Down Counters.
3	Counters with Parallel load, enable, synchronous clear and asynchronous clear. Use of available counters to build counters of different count.
4	Other counters: *Ripple Counter*, Arbitrary Count Sequence.
	***Unit VI* : Memory & PLDs**
1	Memory devices: RAMs & ROMs . Combinational Circuit Implementation with ROM