King Fahd University of Petroleum & Minerals Computer Engineering Dept

COE 341 – Data and Computer Communications

Term 061

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Lecture Contents

1. Asynchronous and Synchronous Transmission
2. Error Detection
3. Error Correction (Optional)

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Timing Requirement

- Reception of digital data requires sampling of received signal at receiver → Sampling time should be known
- Clock drift (example):
  - If a receiver clock drifts by 1% every sample time,
  - Then for $T_b = 1\mu sec$, total drift after 50 bit times = $50 \times 0.01 = 0.5\ \mu sec$
  - Hence, instead of sampling at the middle of the bit time, the receiver will sample at the edge of the bit (I.e. receiver is out-of-synch with transmitter clock)
- For correct reception, receiver clock/carrier should be synchronized with transmitter

Asynchronous Transmission

- Exploits: Rx-er can remain for short period in synch with Tx-er
- Used for short stream of bits – data transmitted one character (5 ~ 8 bits) at a time
- Synchronization is needed to be maintained for the length of short transmission
- Character is delimited (start & end) by known signal elements: start bit – stop element
- Rx-er re-synchs with the arrival of new character

Asynchronous Transmission

- Simple / Cheap
- Efficiency: transmit 1 start bit + 8 bit of data +2 stop bits ➔ Efficiency = 8/11 = 72% (or overhead = 3/11 = 28%)
- Good for data with large gaps (e.g. keyboard, etc)

Receive idle signal

Receive Start bit

Receive Stop element

S1
S2

S1: receiver in idle state
S2: receive is receiving character

Idle state of line

5 to 8 data bits

odd or even parity or unused

Remain idle or next start bit

1 to 2 bit times

0

Start bit

P bit

Stop element

1

(a) Character format

Unpredicatable time interval between characters

Start bit

Stop element

Start bit

Stop element

1 1 0 1 0 0 0 1   0 1 1 0 1 1 0 0

(b) 8-bit asynchronous character stream

Example: Problem 6-5

6-5: An asynchronous transmission scheme uses 8 bits, an even parity, and a stop element of length 2 bits. What percentage of clock inaccuracy can be tolerated at the receiver with respect to the framing error? Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase.

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Example: Problem 6-5 - solution

An accurate clock will start will start in phase (middle of first bit) and end end in phase (middle of last bit)

However, a slow clock (time between two consecutive samples increases) will start in phase but will sample the last bit away from the middle of the actual bit duration – for this not to make a mistake it should sample <u>at most</u> at end of the last bit duration

For a fast clock (time between two consecutive samples decreases) will start in phase but will sample the last bit before the middle of the actual bit duration – for this clock not to make a mistake it should sample <u>at least</u> at beginning of the last bit duration

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Example: Problem 6-5 - solution (2)

Let the bit duration be T. Then a frame is 12T long.

Let a clock period be T'. The last bit (bit 12) is sampled at 11.5T'.

For a fast running clock, the condition to satisfy is

$$11.5T' > 11T \implies \frac{T}{T'} < \frac{11.5}{11} = 1.045 \implies f_{clock} < 1.045 f_{bit}$$

For a slow running clock, the condition to satisfy is
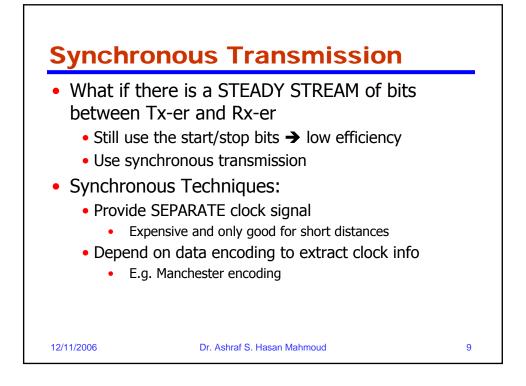
$$11.5T' < 12T \implies \frac{T}{T'} > \frac{11.5}{12} = 0.958 \implies f_{clock} > 0.958 f_{bit}$$
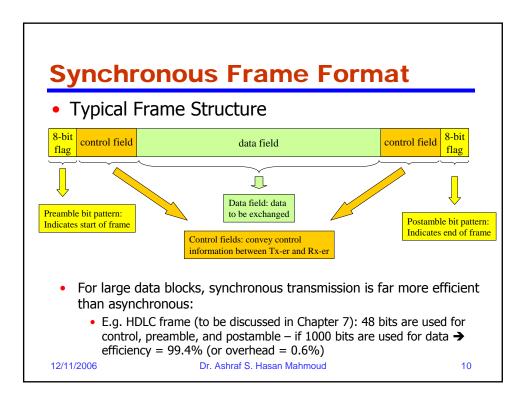
Therefore, the overall condition: $0.958\ f_{bit} < f_{clock} < 1.045\ f_{bit}$

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Synchronous Transmission

- What if there is a STEADY STREAM of bits between Tx-er and Rx-er
  - Still use the start/stop bits ➔ low efficiency
  - Use synchronous transmission
- Synchronous Techniques:
  - Provide SEPARATE clock signal
    - Expensive and only good for short distances
  - Depend on data encoding to extract clock info
    - E.g. Manchester encoding

Synchronous Frame Format

- Typical Frame Structure

8-bit flag	control field	data field	control field	8-bit flag

Preamble bit pattern: Indicates start of frame

Data field: data to be exchanged

Control fields: convey control information between Tx-er and Rx-er

Postamble bit pattern: Indicates end of frame

- For large data blocks, synchronous transmission is far more efficient than asynchronous:
  - E.g. HDLC frame (to be discussed in Chapter 7): 48 bits are used for control, preamble, and postamble – if 1000 bits are used for data ➔ efficiency = 99.4% (or overhead = 0.6%)

Error Detection

$$1 \quad 2 \quad 3 \quad 4 \qquad \ldots \qquad \ldots \qquad F\text{-}2 \ F\text{-}1 \ F$$

$$1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ \ldots \ 0 \ 0 \ 1$$

Prob [1st bit in error] = BER
Prob [1st bit correct] = 1-BER

Prob [2nd bit in error] = BER
Prob [2nd bit correct] = 1-BER

Prob [Fth bit in error] = BER
Prob [Fth bit correct] = 1-BER

$$\text{Prob [k bits in error in frame]} = \binom{F}{k}(BER)^k(1-BER)^{F-k}$$

Error Detection – cont'd

- Hence, for a frame of F bits,

    Prob [frame is correct] = Prob [0 bits in error]
    $\qquad\qquad\qquad\qquad = (1\text{-}BER)^F$

    Prob [frame is erroneous] = Prob[1 OR MORE bits in error]
    $\qquad\qquad\qquad\qquad = 1 - \text{Prob[0 bits in error]}$
    $\qquad\qquad\qquad\qquad = 1 - (1\text{-}BER)^F$
Or

    Prob [frame is erroneous] = Prob [1 bit in error] +
    $\qquad\qquad\qquad\qquad$ Prob[2 bits in error] + … +
    $\qquad\qquad\qquad\qquad$ Prob[F bits in error]
    $\qquad\qquad\qquad\quad = 1 - \text{Prob[0 bits in error]}$
    $\qquad\qquad\qquad\quad = 1 - (1\text{-}BER)^F$

Error Detection (2)

E = f(Data)

Data

Data | E

E, E' = error detecting codes
f = error detecting code function

Receiver

Data | E

E' = f(Data) → Compare

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Cyclic Redundancy Check (CRC)

k-bit block of data (*M*) ⟹ n-bit file check sequence (*F*)

Processing: compute FCS (for some given an n+1 bit polynomial *P*)

| k-bit block of data | N-bit file check sequence |

k+n bit frame to be transmitted = T

- Modulo 2 arithmetic (like XOR) is used to generate the FCS:
  - $0 \pm 0 = 0$; $1 \pm 0 = 1$; $0 \pm 1 = 1$; $1 \pm 1 = 0$
  - $1 \times 0 = 0$; $0 \times 1 = 0$; $1 \times 1 = 1$

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CRC – Mapping Binary Bits into Polynomials

- Consider the following k-bit word or frame and its polynomial equivalent:

$$b_{k-1} \, b_{k-2} \, ... \, b_2 \, b_1 \, b_0 \rightarrow b_{k-1}x^{k-1} + b_{k-2}x^{k-2} + ... + b_1x^1 + b_0$$

where b_i (k-1$\leq$ i $\leq$0) is either 1 or 0

- Example1: an 8 bit word M = 11011001 is represented as $M(x) = x^7+x^6+x^4+x^3+1$

CRC – Mapping Binary Bits into Polynomials - cont'd

- Example2: What is $x^4M(x)$ equal to?

  $x^4M(x) = x^4(x^7+x^6+x^4+x^3+1) = x^{11}+x^{10}+x^8+x^7+x^4$, the equivalent bit pattern is 110110010000 (i.e. four zeros added to the left of the original M pattern)

- Example3: What is $x^4M(x) + (x^3+x+1)$?

  $x^4M(x) + (x^3+x+1) = x^{11}+x^{10}+x^8+x^7+x^4+ x^3+x+1$, the equivalent bit pattern is 110110011011 (i.e. pattern $1011 = x^3+x+1$ added to the left of the original M pattern)

CRC Calculation

- T = (k+n)-bit frame to be tx-ed, n < k
- M = k-bit message, the first k bits of frame T
- F = n-bit FCS, the last n bits of frame T
- P = pattern of n+1 bits (a predetermined divisor)

T = (n+k)-bit frame → | M = k-bit message | F = n-bit FCS |

P =(n+1) bit divisor

Note:
-T(x) is the polynomial (of k+n-1st degree or less) representation of frame T
-M(x) is the polynomial (of k-1st degree or less) representation of message M
- F(x) is the polynomial (of n-1st degree or less) representation of FCS
- P(x) is the polynomial (of nth degree or less) representation of the divisor P
-T(x) = X^n M(x) + F(x) – refer to example 3 on previous slide

CRC Calculation (2)

- <u>Design</u>: frame T such that it divides the pattern P with no remainder?
- <u>Solution</u>: Since the first component of T, M, is the data part, it is required to find F (or the FCS) such that T divides P with no remainder

Using the polynomial equivalent:
T(x) = X^n M(x) + F(x)
One can show that F(x) = remainder of $x^n M(x) / P(x)$
i.e if $x^n M(x) / P(x)$ is equal to Q(x) + R(x)/P(x), then F(X) is set to be equal to R(X).

<u>Note that:</u>

Polynomial of degree k+n
-------------------------------- = polynomial of degree k + remainder polynomial of degree n-1
Polynomial of degree n

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CRC Calculation - Procedure

1. **Shift pattern M n bits to the lift**
2. **Divide the new pattern 2^nM by the pattern P**
3. **The remainder of the division R (n bits) is set to be the FCS**
4. **The desired frame T is 2^nM plus the FCS bits**

> **Note:**
> 2^nM is the pattern resulting from shifting the pattern M n bits to the left. In other words, the polynomial equivalent of the pattern 2^nM is $x^nM(x)$

CRC Calculation – Example

- **Message M = 1010001101 (10 bits) ➔ k = 10**
  Pattern P = 110101 (6 bits – note 0th and nth bits are 1s)
  ➔n + 1 = 6 ➔ n = 5
  Find the frame T to be transmitted?
- **Solution:**

Size of M = k
Size of P = n+1
Size of R or FCS = n
Size of T = n+k

- **FCS = R is equal to 01110**
- **Frame T = 101000110101110**
- **As an exercise, verify that T divided by P has no remainder**

R (note a zero is added to the left to make n bits)

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CRC Calculation – The previous example BUT using Polynomials

- Message M = 1010001101 (10 bits) ➔ k = 10
- M(x) = $x^9 + x^7 + x^3 + x^2 + 1$ ➔ $x^5M(x) = x^{14} + x^{12} + x^8 + x^7 + x^5$
- Pattern P = 110101 (6 bits – note 0th and nth bits are 1s) ➔ n + 1 = 6 ➔ n = 5
- P(x) = $x^5 + x^4 + x^2 + 1$
- Find the frame T to be transmitted?
- Solution:

$$
\begin{array}{r}
x^9 +x^8 \quad +x^6 \quad +x^4 \quad +x^2 +x \\
\hline
x^5 +x^4 +x^2 +1 \, \big) \, x^{14} \quad +x^{12} \qquad +x^8 +x^7 \quad +x^5 \\
x^{14} +x^{13} \quad +x^{11} \quad +x^9 \\
\hline
x^{13} +x^{12} +x^{11} \quad +x^9 +x^8 +x^7 \quad +x^5 \\
x^{13} +x^{12} \quad +x^{10} \quad +x^8 \\
\hline
x^{11} +x^{10} +X^9 \quad +x^7 \quad +x^5 \\
x^{11} +x^{10} \quad +X^8 \quad +x^6 \\
\hline
x^9 +x^8 +x^7 +x^6 +x^5 \\
X^9 +x^8 \quad +x^6 \quad +x^4 \\
\hline
+x^7 \quad +x^5 +x^4 \\
+x^7 +x^6 \quad +x^4 \quad +x^2 \\
\hline
x^6 +x^5 \quad +x^2 \\
x^6 +x^5 \quad +x^3 \quad +x \\
\hline
+x^3 +x^2 +x
\end{array}
$$

- FCS = R(x) = $x^3 + x^2 + x$
  (or $0x^4 + x^3 + x^2 + x$)
- ➔ R is equal to 01110
- Frame T = 101000110101110
- As an exercise, verify that T divided by P has no remainder

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CRC Calculation – The previous example BUT using Polynomials – cont'd

- Message M = 1010001101 (10 bits)
- ➔ M(x) = $x^9 + x^7 + x^3 + x^2 + 1$
- ➔ ➔ $x^5M(x) = x^{14} + x^{12} + x^8 + x^7 + x^5$
- Pattern P = 110101
- ➔ P(x) = $x^5 + x^4 + x^2 + 1$
- R(x) = $x^3 + x^2 + x$
- Q(x) = $x^9 + x^8 + x^6 + x^4 + x^2 + x$
- T(X) = $x^5M(x) + R(x)$
  = $x^{14} + x^{12} + x^8 + x^7 + x^5 + x^3 + x^2 + x$, or
  T = 101000110101110

- <u>Exercise</u>: Verify that Q(x) P(x) + R(x) = $x^5 M(x)$

Example: Problem 6-12

6-12: for P=110011 and M = 11100011, find the CRC

```
                                    10110110
                    110011/1110001100000
                           110011
                            101111
                            110011
                             111000
                             110011
                              101100
                              110011
                               111110
                               110011
                          CRC =    11010
```

CRC – Receiver Procedure

- **Tx-er transmits frame T**
- **Channel introduces error pattern E**
- **Rx-er receives frame T_r = T⊕E** (note that if E = 000..000, then Tr is equal to T, i.e. error free transmission)
- **T_r is divided by P, Remainder of division is R**
- **if R is ZERO, Rx-er assumes no errors in frame; else Rx-er assumes erroneous frame**
- **If an error occurs and T_r is still divisible by P ➔ UNDETECTABLE error** (this means the E is also divisible by P)

CRC – Transmitter Circuit

= 1-bit shift register   ⊕ = Exclusive-OR circuit

Shift register circuit for dividing by $P = X^5+X^4+X^2+1$

(a) Shift-register implementation

	C_4	C_3	C_2	C_1	C_0	$C_4 \oplus C_3$	$C_4 \oplus C_1$	$C_4 \oplus input$	input	
Initial	0	0	0	0	0	0	0	1	1	
Step1	0	0	0	0	1	0	0	0	0	
Step2	0	0	0	1	0	0	1	1	1	
Step3	0	0	1	0	1	0	0	0	0	
Step4	0	1	0	1	0	1	1	0	0	Message to be sent
Step5	1	0	1	0	0	1	1	1	0	
Step6	1	1	1	0	1	0	1	0	1	
Step7	0	1	1	1	0	1	1	1	1	
Step8	1	1	1	0	1	0	1	1	0	
Step9	0	1	1	1	1	1	1	1	1	
Step10	1	1	1	1	1	0	0	1	0	
Step11	0	1	0	1	1	1	1	0	0	
Step12	1	0	1	1	0	1	0	1	0	Five zeros added
Step13	1	1	0	0	1	0	1	1	0	
Step14	0	0	1	1	1	0	1	0	0	
Step15	0	1	1	1	0	1	1	0	—	

(b) Example with input of 1010001101

CRC – Receiver Circuit

- **Tx-er transmits frame T**

Figure 7.7 General CRC Architecture to Implement Divisor
$$1 + A_1X + A_2X^2 + \dots + A_{n-1}X^{n-1} + X^n$$

Cyclic Redundancy Check (CRC)

- Animation for CRC Calculation

Example: Problem 6-13

A CRC is constructed to generate a 4-bit FCS for an 11-bit message. The generator polynomial is X^4+X^3+1

a) Draw the shift register circuit that would perform this task (see figure 6.5)

b) Encode the data bit sequence 10011011100 (leftmost bit is the LSB) using the generator polynomial and give the code word

c) Now assume that bit 7 (counting from the LSB) in the code word is in error and show that the detection algorithm detects the error

Example: Problem 6-13 - solution

a)

C_3 ← ⊕ ← C_2 ← C_1 ← C_0 ← ⊕ ← Input data

Example: Problem 6-13 - solution

b)

```
                    0 0 1 0 1 1 1 0 1 0 0   ⇐ Q(X)
1 1 0 0 1 0 0 1 1 1 0 1 1 0 0 1 0 0 0 0   ⇐ X⁴M(X)
          1 1 0 0 1
          1 0 0 1 0
          1 1 0 0 1
            1 0 1 1 0
            1 1 0 0 1
              1 1 1 1 1
              1 1 0 0 1
                1 1 0 0 0
                1 1 0 0 1
                  0 1 0 0
```

⇐ P

$M(X) = X^8 + X^7 + X^6 + X^4 + X^3 + 1$
$P(X) = X^4 + X^3 + 1$

Size of M = 11
Size of P = 4+1= 5
Size of R or FCS = 4
Size of T = 4+11=15

➔ R = 0 1 0 0 or $R(X) = X^2$

Transmitted Frame T = 001110110010100

$T(X) = X^4 M(X) + R(X) = X^{12}+X^{11}+X^{10}+X^8+X^7+X^4+X^2$

Notes:

1. $X^4 M(X)/P(X) = Q(X) + R(X)/P(X)$, where $Q(X) = X^8 + X^6 + X^5 + X^4 + X^2$ (as seen from the long division process)

2. One can verify that $P(X) Q(X) + R(X)$ is indeed equal to $X^4 M(X)$ {note that for the addition of polynomial terms modulo-2 applies; i.e. $X^9 + X^9 = 0$}

Example: Problem 6-13 - solution

c) Received frame (LSB from the left) = 0 0 1 0 1 0 <u>0</u> 0 0 1 0 1 1 1 0 0
dividing by P yields a nonzero remainder ➔ error is detected
Remainder = 0111

```
                              0 0 1 0 1 1 1 1 0 1 1
          1 1 0 0 1 | 0 0 1 1 1 0 1 0 0 0 1 0 1 0 0    ⇐  RECEIVED FRAME
                          1 1 0 0 1
              ⇑           1 0 0 0 0
              P           1 1 0 0 1
                            1 0 0 1 0
                            1 1 0 0 1
                              1 0 1 1 1
                              1 1 0 0 1
                                1 1 1 0 0
                                1 1 0 0 1
                                    1 0 1 1 0
                                    1 1 0 0 1
                                      1 1 1 1 0
                                      1 1 0 0 1
                                          1 1 1    ⇐
```

NON ZERO REMAINDER

Textbook Problems of INTEREST

- Texbook Problems list: