

King Fahd University of Petroleum & Minerals Computer Engineering Dept

**COE 342 – Data and Computer
Communications**

Term 032

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Lecture Contents

1. Asynchronous and Synchronous Transmission
2. Line Configuration
 - a. Topology
 - b. Full/Half Duplex
3. Interfacing
 - a. V.24/EIA-232-F
 - b. ISDN Physical Interface

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Timing Requirement

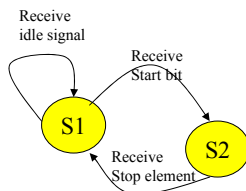
- Reception of digital data requires sampling of received signal at receiver → Sampling time should be known
- Clock drift (example):
 - If a receiver clock drifts by 1% every sample time,
 - Then for $T_b = 1\mu\text{sec}$, total drift after 50 bit times = $50 \times 0.01 = 0.5\mu\text{sec}$
 - Hence, instead of sampling at the middle of the bit time, the receiver will sample at the edge of the bit (I.e. receiver is out-of-synch with transmitter clock)
- For correct reception, receiver clock/carrier should be synchronized with transmitter

Asynchronous Transmission

- Exploits: Rx-er can remain for short period in synch with Tx-er
- Used for short stream of bits – data transmitted one character (5 ~ 8 bits) at a time
- Synchronization is needed to be maintained for the length of short transmission
- Character is delimited (start & end) by known signal elements: start bit – stop element
- Rx-er re-synchs with the arrival of new character

Asynchronous Transmission

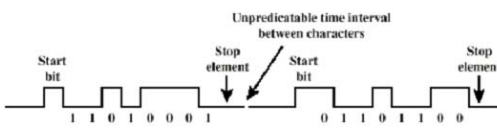
- Simple / Cheap
- Efficiency: transmit 1 start bit + 8 bit of data + 2 stop bits → Efficiency = $8/11 = 72\%$ (or overhead = $3/11 = 28\%$)
- Good for data with large gaps (e.g. keyboard, etc)



S1: receiver in idle state
S2: receiver is receiving character



(a) Character format



(b) 8-bit asynchronous character stream

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Example: Problem 6-5

6-5: An asynchronous transmission scheme uses 8 bits, an even parity, and a stop element of length 2 bits. What percentage of clock inaccuracy can be tolerated at the receiver with respect to the framing error? Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase.

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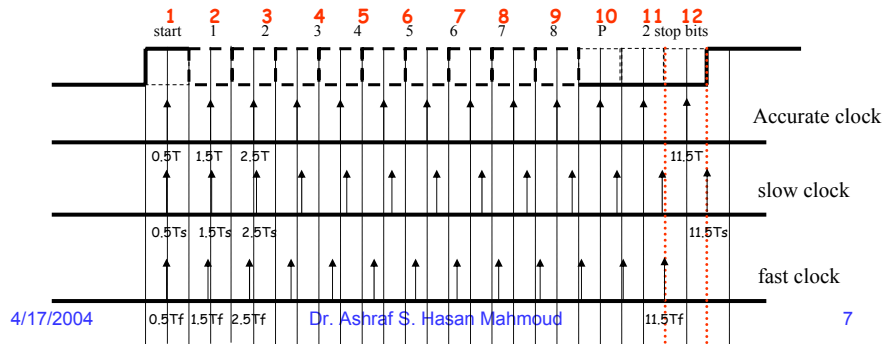
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Example: Problem 6-5- solution

An accurate clock will start in phase (middle of first bit) and end in phase (middle of last bit)

However, a slow clock (time between two consecutive samples increases) will start in phase but will sample the last bit away from the middle of the actual bit duration – for this not to make a mistake it should sample at most at end of the last bit duration

For a fast clock (time between two consecutive samples decreases) will start in phase but will sample the last bit before the middle of the actual bit duration – for this clock not to make a mistake it should sample at least at beginning of the last bit duration



Example: Problem 6-5 - solution (2)

Let the bit duration be T . Then a frame is $12T$ long.

Let a clock period be T' . The last bit (bit 12) is sampled at $11.5T'$.

For a fast running clock, the condition to satisfy is

$$11.5T' > 11T \Rightarrow \frac{T}{T'} < \frac{11.5}{11} = 1.045 \Rightarrow f_{clock} < 1.045 f_{bit}$$

For a slow running clock, the condition to satisfy is

$$11.5T' < 12T \Rightarrow \frac{T}{T'} > \frac{11.5}{12} = 0.958 \Rightarrow f_{clock} > 0.958 f_{bit}$$

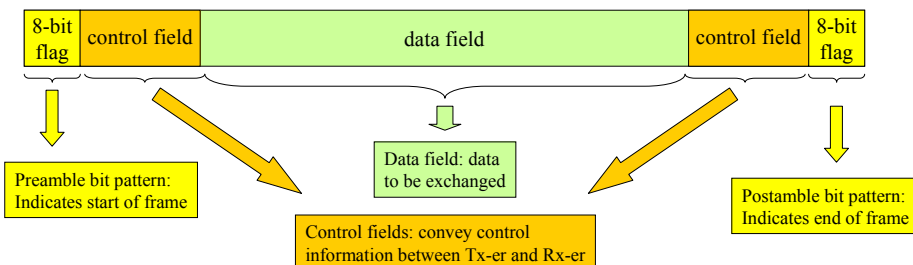
Therefore, the overall condition: $0.958 f_{bit} < f_{clock} < 1.045 f_{bit}$

Synchronous Transmission

- What if there is a STEADY STREAM of bits between Tx-er and Rx-er
 - Still use the start/stop bits → low efficiency
 - Use synchronous transmission
- Synchronous Techniques:
 - Provide SEPARATE clock signal
 - Expensive and only good for short distances
 - Depend on data encoding to extract clock info
 - E.g. Manchester encoding

Synchronous Frame Format

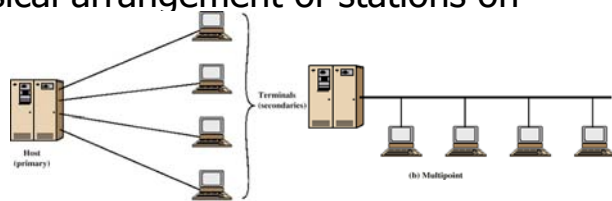
- Typical Frame Structure



- For large data blocks, synchronous transmission is far more efficient than asynchronous:
 - E.g. HDLC frame (to be discussed in Chapter 7): 48 bits are used for control, preamble, and postamble – if 1000 bits are used for data → efficiency = 99.4% (or overhead = 0.6%)

Line Configuration

- Full Duplex: Simultaneous transmission and reception
 - Requires two data paths but not necessarily two physical connections or lines
- Half Duplex: one direction active only at any one time
- Topology: Physical arrangement of stations on medium
 - Point-to-Point
 - Multipoint:



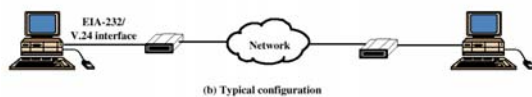
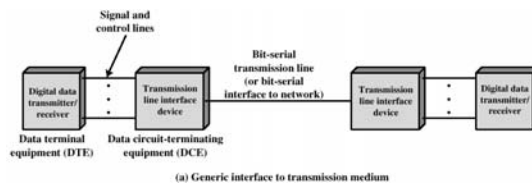
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Interfacing

- Data Terminal Equipment (DTE): terminals or computers
- Data Circuit Equipment (DCE): modem
- Two DCEs exchanging data on behalf of DTEs must use exact same protocol



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DTE-DCE Interface Definition

- Mechanical: physical specification of connection – type, dimensions, location of pins, etc
- Electrical: voltage levels and timing signals used
- Functional: specify functions that are performed for circuits – rx circuit, tx circuit, etc.
- Procedural: specification of sequence of event for transmitting data based on functional specification
- Two examples:
 - V.24/EIA-232-F, and
 - ISDN physical interface

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V.24/EIA-232-F

- Previously known as RS-232
- Used to connection DTE to voice-grade modem
 - This is the connection used to connect a PC to an external modem using the COM port

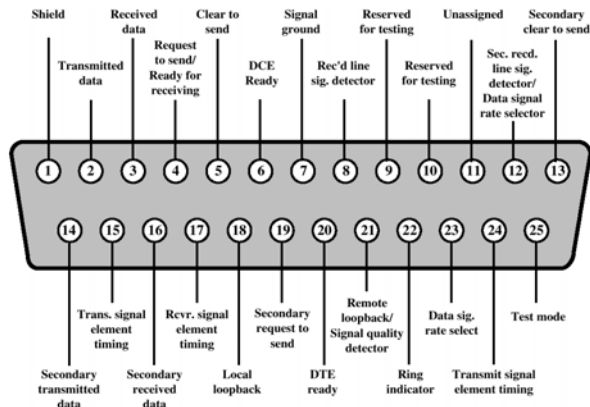
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V.24/EIA-232-F - Mechanical Specification

- 25-pin connector
- In most applications – far less than 25 pins are used
- Pin assignment is shown in figure



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V.24/EIA-232-F - Electrical Specification

- Digital signaling is used on all circuits
- Depending on the function of the circuit, electrical value is interpreted as binary data or control signal
- Voltage levels (data/Control):
 - Common ground – 0 volts
 - < -3 Volts – binary 1/OFF signal
 - > +3 Volts – binary 0/ON signal
- Assumes NRZ-L signal
- Appropriate for R < 20 kb/s and distance < 15 meters

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V.24/EIA-232-F - Functional Specification

- Table 6.1
- Circuits:
 - Data
 - Control
 - Timing
 - Ground
- There is one primary data circuit per direction – full duplex is possible
- There are secondary data circuits too

V.24/EIA-232-F - Procedural Specification

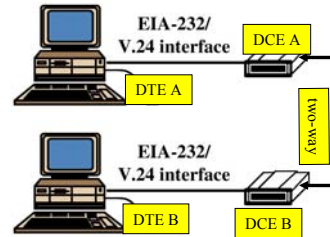
- Defines the sequence in which the various circuits are used for a particular application

V.24/EIA-232-F - Procedural Specification – Examples

- **Example 1: Asynchronous private line modem**
 - Two terminals (computers) connected back to back through modems (no telephone network)

- **Interchange Circuits Needed:**

- Signal Ground (102)
- Transmitted Data (103)
- Received Data (104)
- Request to Send (105)
- Clear to Send (106)
- DCE Ready (107)
- Received Line Signal Detector (109)



- **Sequence:**(DTE A sends a character to DTE B)

1. When DCE A is ready (e.g. turned on) → DCE Ready (107) ON
2. When DTE A has data to send → Request to Send (105) ON
3. DCE A responds → Clear to Send (106) ON
4. DTE A now sends data → Transmitted Data (103)
5. When DCE B receives data → Received Line Signal Detector (109)
6. DCE B deliver data to DTE B → Received Data (104)

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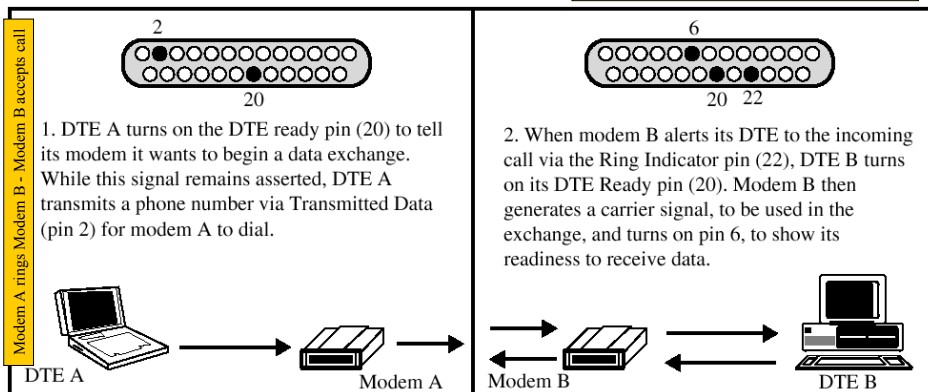
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V.24/EIA-232-F - Procedural Specification – Examples (2)

- **Example 2-1: Two terminals exchanging data across a telephone network**

In addition to previous interchange circuits:
 -DTE Ready (108.2)
 -Ring Indicator (125)



Modem A rings Modem B - Modem B accepts call

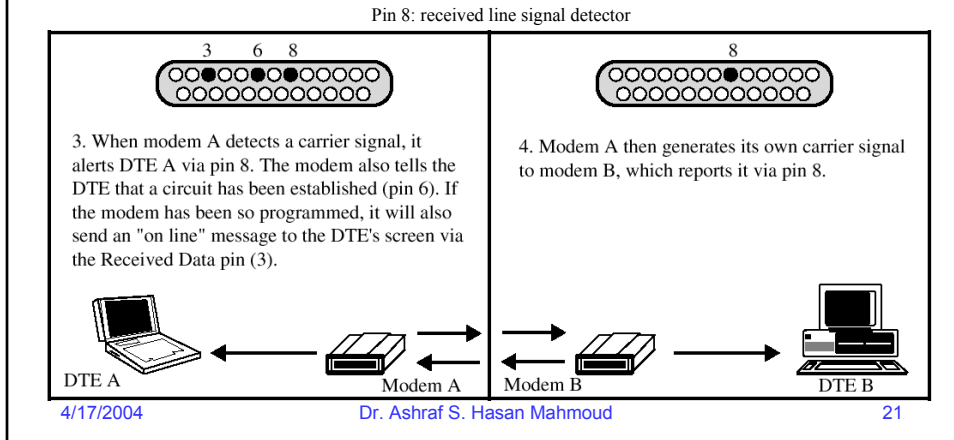
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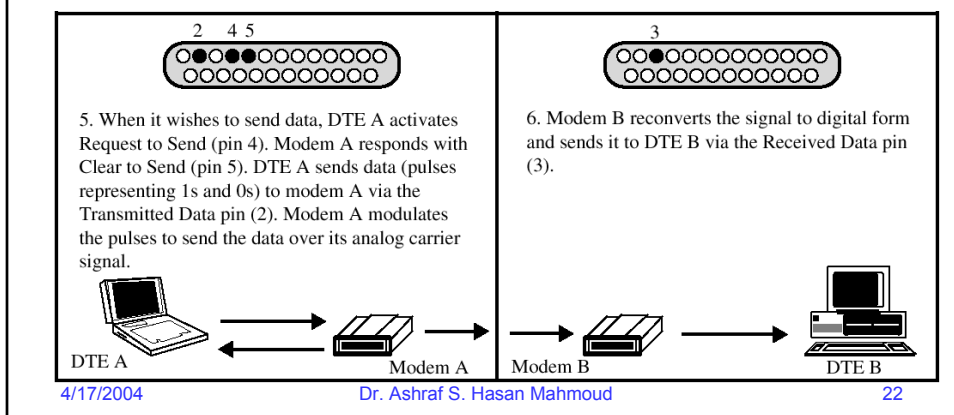
V.24/EIA-232-F - Procedural Specification – Examples (3)

- Example 2-2: Modem A confirms the connection to DTE A and also generates a carrier for Modem B



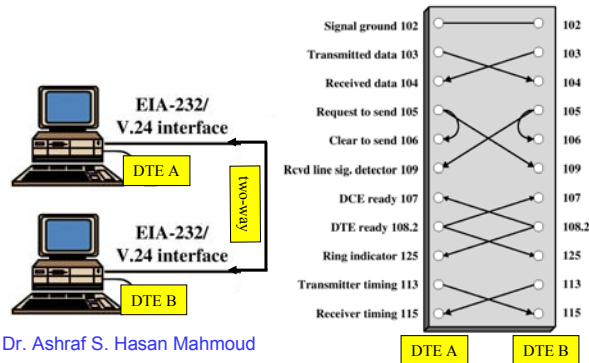
V.24/EIA-232-F - Procedural Specification – Examples (4)

- Example 2-3: Data exchange phase – DTE sends data to Modem A – Modem A modulate and transmit to Modem B – Modem B recovers data and sends to DTE B



V.24/EIA-232-F - Procedural Specification – Examples (5)

- Example 3: Two terminals connected back-to-back through the V.24 interface BUT with no DCEs
- This is referred to as the NULL modem connection
- For short distance connections



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ISDN Physical Interface

- V.24/EIA232-F provides many functionalities using the large number of circuits (expensive)
- Build fewer circuits but more logic into DTE and DCE – Examples:
 - X.21 standard used to interface to public circuit-switched networks uses 15-pin connection)
 - ISND physical interface uses 8-pin connection

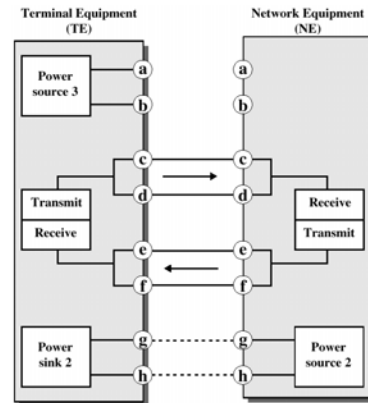
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ISDN Physical Interface (2)

- ISDN Terminology:
 - TE: Terminal equipment (equivalent to DTE)
 - NE: Network equipment (equivalent to DCE or point of connection to network)
- Two pins for exchanging data and control for each direction (Note TE and NE need to make the right interpretation of signal!)
- May allow to transfer power



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ISDN Physical Interface – Electrical Specification

- Balanced Transmission*:
 - Signal transmitted as a current – *Differential Signaling*
 - Binary value – direction of current
- Balanced Transmission is more resistant to interference and produces less noise
- Basic rate of 192 kb/s – Pseudoternary coding: 1 no signal, 0 is +ve/-ve pulse of 750 mV +/- 10%
- Primary rate (two options)
 - 1.544 Mb/s – AMI with B8ZS and
 - 2.048 Mb/s – AMI with HDB3

* EIA-232 uses UNBALANCED transmission where a single conductor carries the signal, with ground providing the current return path

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Textbook Problems of INTEREST

- Textbook Problems list: 6-1, 6-2, 6-5, 6-6, 6-20