King Fahd University of Petroleum & Minerals Computer Engineering Dept

COE 342 – Data and Computer Communications

Term 021

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Lecture Contents

1. Asynchronous and Synchronous Transmission
2. Line Configuration
   a. Topology
   b. Full/Half Duplex
3. Interfacing
   a. V.24/EIA-232-F
   b. ISDN Physical Interface
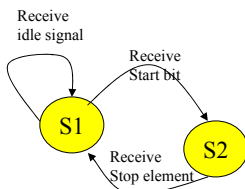
Timing Requirement

- Reception of digital data requires sampling of received signal at receiver → Sampling time should be known
- Clock drift (example):
  - If a receiver clock drifts by 1% every sample time,
  - Then for Tb = 1μsec, total drift after 50 bit times = 50 X 0.01 = 0.5 μsec
  - Hence, instead of sampling at the middle of the bit time, the receiver will sample at the edge of the bit (I.e. receiver is out-of-synch with transmitter clock)
- For correct reception, receiver clock/carrier should be synchronized with transmitter

Asynchronous Transmission

- Exploits: Rx-er can remain for short period in synch with Tx-er
- Used for short stream of bits – data transmitted one character (5 ~ 8 bits) at a time
- Synchronization is needed to be maintained for the length of short transmission
- Character is delimeted (start & end) by known signal elements: start bit – stop element
- Rx-er re-synchs with the arrival of new character
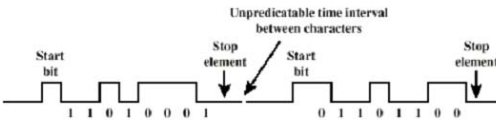
Asynchronous Transmission

- Simple / Cheap
- Efficiency: transmit 1 start bit + 8 bit of data +2 stop bits ➔ Efficiency = 8/11 = 72% (or overhead = 3/11 = 28%)
- Good for data with large gaps (e.g. keyboard, etc)

Receive idle signal

Receive Start bit

S1

S2

Receive Stop element

S1: receiver in idle state
S2: receive is receiving character

Idle state of line

5 to 8 data bits

odd or even parity or unused

Remain idle or next start bit

1 to 2 bit times

0

1

Start bit

P bit

Stop element

(a) Character format

Unpredictable time interval between characters

Start bit

Stop element

Start bit

Stop element

1 1 0 1 0 0 0 1

0 1 1 0 1 1 0 0

(b) 8-bit asynchronous character stream

Example: Problem 6-5

6-5: An asynchronous transmission scheme uses 8 bits, an even parity, and a stop element of length 2 bits. What percentage of clock inaccuracy can be tolerated at the receiver with respect to the framing error? Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase.
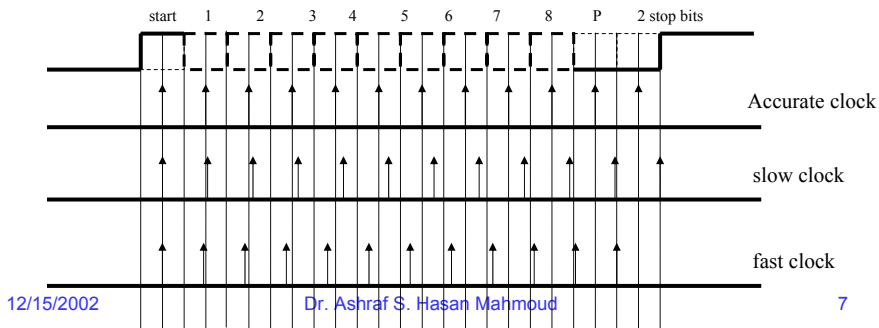
Example: Problem 6-5 - solution

An accurate clock will start will start in phase (middle of first bit) and end end in phase (middle of last bit)

However, a slow clock (time between two consecutive samples increases) will start in phase but will sample the last bit away from the middle of the actual bit duration – for this not to make a mistake it should sample <u>at most</u> at end of the last bit duration

For a fast clock (time between two consecutive samples decreases) will start in phase but will sample the last bit before the middle of the actual bit duration – for this clock not to make a mistake it should sample <u>at least</u> at beginning of the last bit duration

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Example: Problem 6-5   - solution (2)

Let the bit duration be T. Then a frame is 12T long.

Let a clock period be T'. The last bit (bit 12) is sampled at 11.5T'.

For a fast running clock, the condition to satisfy is

$$11.5T' > 11T \implies \frac{T}{T'} < \frac{11.5}{11} = 1.045 \implies f_{clock} < 1.045 f_{bit}$$

For a slow running clock, the condition to satisfy is

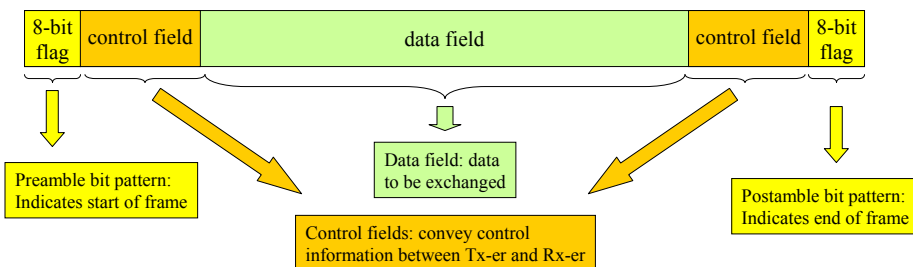$$11.5T' < 12T \implies \frac{T}{T'} > \frac{11.5}{12} = 0.958 \implies f_{clock} > 0.958 f_{bit}$$

Therefore, the overall condition: 0.958 f_{bit} < f_{clock} <1.045 f_{bit}

Synchronous Transmission

- What if there is a STEADY STREAM of bits between Tx-er and Rx-er
  - Still use the start/stop bits ➔ low efficiency
  - Use synchronous transmission
- Synchronous Techniques:
  - Provide SEPARATE clock signal
    - Expensive and only good for short distances
  - Depend on data encoding to extract clock info
    - E.g. Manchester encoding

Synchronous Frame Format

- Typical Frame Structure

8-bit flag	control field	data field	control field	8-bit flag

Preamble bit pattern: Indicates start of frame

Data field: data to be exchanged

Control fields: convey control information between Tx-er and Rx-er

Postamble bit pattern: Indicates end of frame

- For large data blocks, synchronous transmission is far more efficient than asynchronous:
  - E.g. HDLC frame (to be discussed in Chapter 7): 48 bits are used for control, preamble, and postamble – if 1000 bits are used for data ➔ efficiency = 99.4% (or overhead = 0.6%)

Line Configuration

- Full Duplex: Simultaneous transmission and reception
  - Requires two data paths but not necessarily two physical connections or lines
- Half Duplex: one direction active only at any one time
- Topology: Physical arrangement of stations on medium
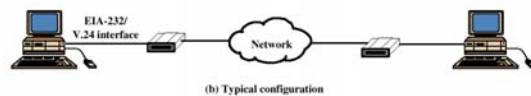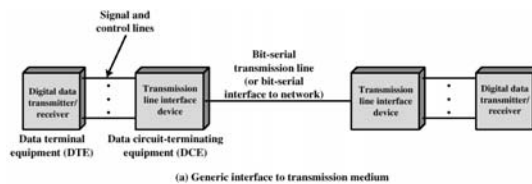 - Point-to-Point
  - Multipoint:
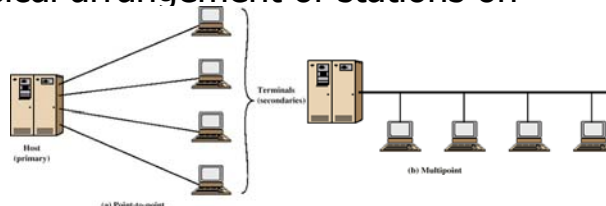
Interfacing

- Data Terminal Equipment (DTE): terminals or computers
- Data Circuit Equipment (DCE): modem

- Two DCEs exchanging data on behalf of DTEs must use exact same protocol

DTE-DCE Interface Definition

- Mechanical: physical specification of connection – type, dimensions, location of pins, etc
- Electrical: voltage levels and timing signals used
- Functional: specify functions that are performed for circuits – rx circuit, tx circuit, etc.
- Procedural: specification of sequence of event for transmitting data based on functional specification
- Two examples:
  - V.24/EIA-232-F, and
  - ISDN physical interface

V.24/EIA-232-F

- Previously known as RS-232
- Used to connection DTE to voice-grade modem
  - This is the connection used to connect a PC to an external modem using the COM port
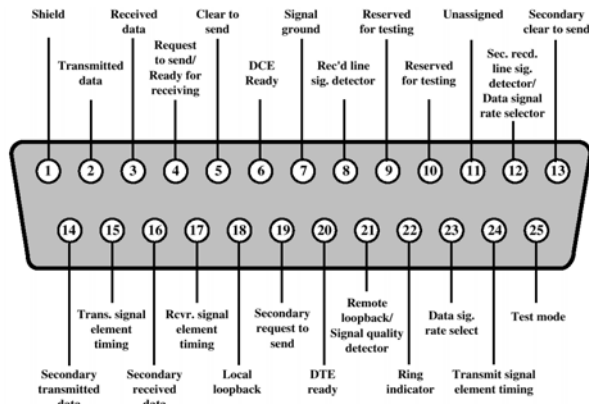
V.24/EIA-232-F - Mechanical Specification

- 25-pin connector
- In most applications – far less than 25 pins are used
- Pin assignment is shown in figure

V.24/EIA-232-F - Electrical Specification

- Digital signaling is used on all circuits
- Depending on the function of the circuit, electrical value is interpreted as binary data or control signal
- Voltage levels (data/Control):
  - Common ground – 0 volts
  - < -3 Volts – binary 1/OFF signal
  - > +3 Volts – binary 0/ON signal
- Assumes NRZ-L signal
- Appropriate for R < 20 kb/s and distance < 15 meters

V.24/EIA-232-F - Functional Specification

- Table 6.1
- Circuits:
  - Data
  - Control
  - Timing
  - Ground
- There is one primary data circuit per direction – full duplex is possible
- There are secondary data circuits too

# V.24/EIA-232-F - Procedural Specification

- Defines the sequence in which the various circuits are used for a particular application

V.24/EIA-232-F - Procedural Specification –Examples

- Example 1: Asynchronous private line modem
  - Two terminals (computers) connected back to back through modems (no telephone network)
- Interchange Circuits Needed:
  a. Signal Ground (102)
  b. Transmitted Data (103)
  c. Received Data (104)
  d. Request to Send (105)
  e. Clear to Send (106)
  f. DCE Ready (107)
  g. Received Line Signal Detector (109)
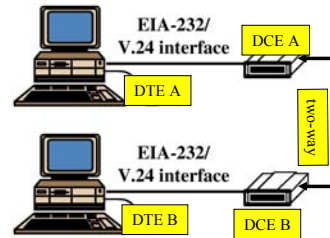
- Sequence:(DTE A sends a character to DTE B)
  1. When DCE A is ready (e.g. turned on)➔ DCE Ready (107) ON
  2. When DTE A has data to send ➔ Request to Send (105) ON
  3. DCE A responds ➔ Clear to Send (106) ON
  4. DTE A now sends data ➔ Transmitted Data (103)
  5. When DCE B receives data ➔ Received Line Signal Detector (109)
  6. DCE B deliver data to DTE B ➔ Received Data (104)

V.24/EIA-232-F - Procedural Specification – Examples (2)

- Example 2-1: Two terminals exchanging data across a telephone network

In addition to previous interchange circuits:
-DTE Ready (108.2)
-Ring Indicator (125)

1. DTE A turns on the DTE ready pin (20) to tell its modem it wants to begin a data exchange. While this signal remains asserted, DTE A transmits a phone number via Transmitted Data (pin 2) for modem A to dial.

2. When modem B alerts its DTE to the incoming call via the Ring Indicator pin (22), DTE B turns on its DTE Ready pin (20). Modem B then generates a carrier signal, to be used in the exchange, and turns on pin 6, to show its readiness to receive data.

Modem A rings Modem B - Modem B accepts call

DTE A   Modem A   Modem B   DTE B

V.24/EIA-232-F - Procedural Specification – Examples (3)

- <u>Example 2-2:</u> Modem A confirms the connection to DTE A and also generates a carrier for Modem B
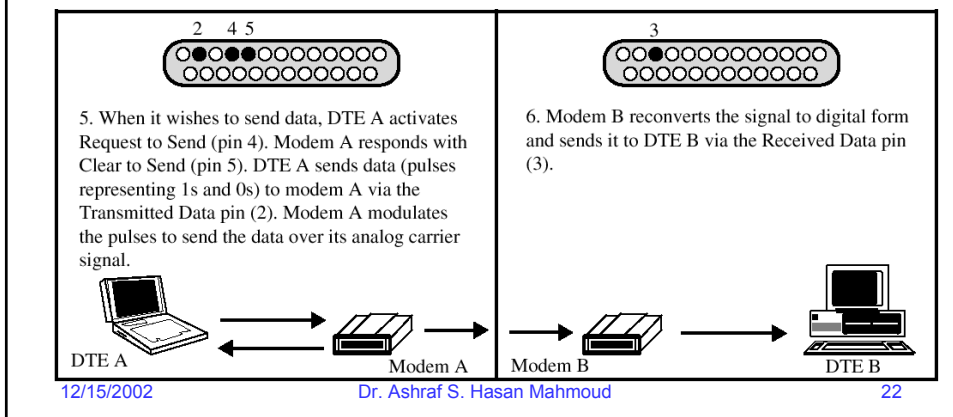
3. When modem A detects a carrier signal, it alerts DTE A via pin 8. The modem also tells the DTE that a circuit has been established (pin 6). If the modem has been so programmed, it will also send an "on line" message to the DTE's screen via the Received Data pin (3).

DTE A   Modem A   Modem B   DTE B

4. Modem A then generates its own carrier signal to modem B, which reports it via pin 8.
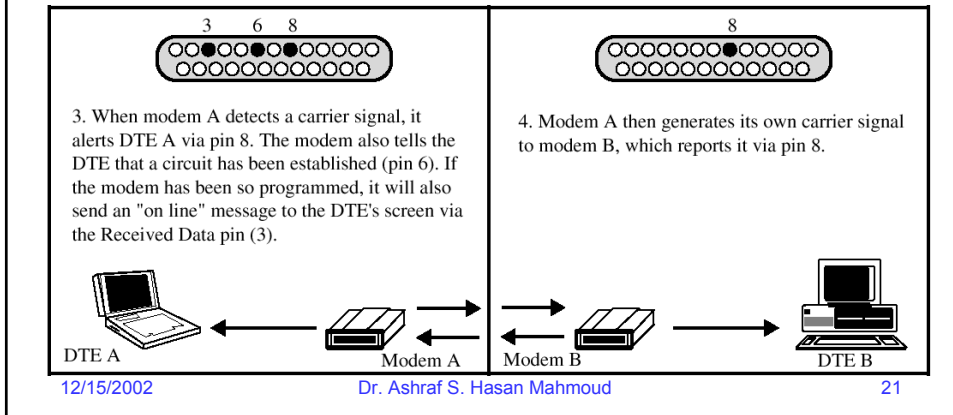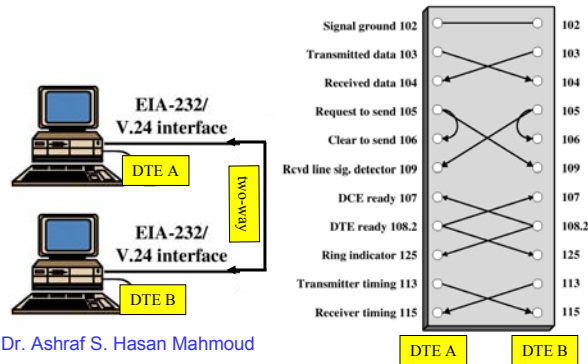

V.24/EIA-232-F - Procedural Specification – Examples (4)

- <u>Example 2-3:</u> Data exchange phase – DTE sends data to Modem A – Modem A modulate and transmit to Modem B – Modem B recovers data and sends to DTE B

5. When it wishes to send data, DTE A activates Request to Send (pin 4). Modem A responds with Clear to Send (pin 5). DTE A sends data (pulses representing 1s and 0s) to modem A via the Transmitted Data pin (2). Modem A modulates the pulses to send the data over its analog carrier signal.

DTE A   Modem A   Modem B   DTE B

6. Modem B reconverts the signal to digital form and sends it to DTE B via the Received Data pin (3).

V.24/EIA-232-F - Procedural Specification – Examples (5)

- Example 3: Two terminals connected back-to-back through the V.24 interface BUT with no DCEs

- This is referred to as the NULL modem connection

- For short distance connections

EIA-232/
V.24 interface

DTE A

two-way

EIA-232/
V.24 interface

DTE B

Signal ground 102		102
Transmitted data 103		103
Received data 104		104
Request to send 105		105
Clear to send 106		106
Rcvd line sig. detector 109		109
DCE ready 107		107
DTE ready 108.2		108.2
Ring indicator 125		125
Transmitter timing 113		113
Receiver timing 115		115

DTE A   DTE B

ISDN Physical Interface

- V.24/EIA232-F provides many functionalities using the large number of circuits (expensive)

- Build fewer circuits but more logic into DTE and DCE – Examples:
  - X.21 standard used to interface to public circuit-switched networks uses 15-pin connection)
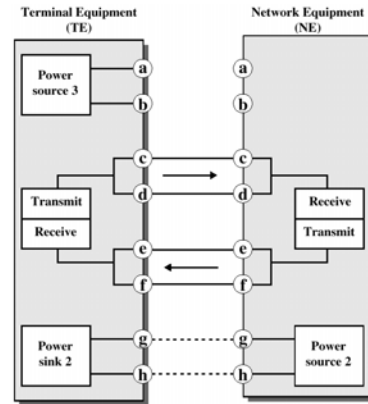 - ISND physical interface uses 8-pin connection

ISDN Physical Interface (2)

- ISDN Terminology:
  - TE: Terminal equipment (equivalent to DTE)
  - NE: Network equipment (equivalent to DCE or point of connection to network)

- Two pins for exchanging data and control for each direction (Note TE and NE need to make the right interpretation of signal!)
- May allow to transfer power

ISDN Physical Interface – Electrical Specification

- Balanced Transmission*:
  - Signal transmitted as a current – *Differential Signaling*
  - Binary value – direction of current
- Balanced Transmission is more resistant to interference and produces less noise
- Basic rate of 192 kb/s – Pseudoternary coding: 1 no signal, 0 is +ve/-ve pulse of 750 mV +- 10%
- Primary rate (two options)
  - 1.544 Mb/s – AMI with B8ZS and
  - 2.048 Mb/s – AMI with HDB3

* EIA-232 uses UNBALANCED transmission where a single conductor carries the signal, with ground providing the current return path

Textbook Problems of INTEREST

- Texbook Problems list: 6-1, 6-2, 6-5, 6-6, 6-8

* EIA-232 uses UNBALANCED transmission where a single conductor carries the signal, with ground providing the current return path