ICS 233
COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

SPRING 2007-08 **Term 072**

Section 2 **Location : 24/178**

Day & Time : UT 11.00 – 12.15 P.M.

Instructor : Dr. Abdul Rahim Naseer

ICS 233
COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

SYLLABUS

COURSE OBJECTIVES

- **Towards the end of this course, students should be able to:**
  - Describe the instruction set architecture of a MIPS processor
  - Analyze, write, and test MIPS assembly language programs

COURSE OBJECTIVES

- **Towards the end of this course, students should be able to:**
  - Describe the organization/operation of integer and floating-point arithmetic units

COURSE OBJECTIVES

- **Towards the end of this course, students should be able to:**
  - Design the datapath and control of a single-cycle processor
  - Design the datapath and control of a pipelined processor and handle hazards

COURSE OBJECTIVES

- **Towards the end of this course, students should be able to:**
  - Describe the organization/operation of memory and caches
  - Analyze the performance of processors and caches

Catalog Description

- **Machine organization;**
- **Assembly language: addressing, stacks, argument passing, arithmetic operations, decisions, modularization;**
- **Input/Output Operations and Interrupts;**
- **Memory Hierarchy and Cache memory;**
- **Pipeline Design Techniques;**
- **Super-scalar architecture;**
- **Parallel Architectures.**

Prerequisite : COE 202, ICS 201

Text Book

- **Computer Organization and Design : The Hardware/ Software Interface**, David A. Patterson and John L. Hennessey, Morgan Kaufmann, Third Edition 2005
- **MIPS Assembly Language Programming**, Robert L. Britton, Pearson Prentice Hall, 2004

Reference Books/Manuals

- **Sivarama P. Dandamudi, "Guide to RISC Processors for Programmers and Engineers", Springer Science, 2005, ISBN 0-387-21017-2**
- **MIPS32 Architecture for Programmers, Volume I: Introduction to the MIPS32 Architecture, MIPS Technologies Inc, Revision 2.50, July 2005.**
- **MIPS32 Architecture for Programmers, Volume II: The MIPS32 Instruction Set, MIPS Technologies Inc, Revision 2.50, July 2005.**
- **MIPS32 Architecture for Programmers, Volume III: The MIPS32 Privileged Resource Architecture, MIPS Technologies Inc, Revision 2.50, July 2005.**

Course Topics & Lecture Breakdown

Week	Course Topics	Topic Reference in the Text Book
1	Introduction to computer architecture, assembly and machine languages, components of a computer system, memory hierarchy, instruction execution cycle, chip manufacturing process, technology trends, programmer's view of a computer system.	Chapter 1
2 , 3	Instruction set design, RISC design principles, MIPS registers, instruction formats, arithmetic instructions, immediate operands, bit manipulation, load and store instructions, byte ordering, addressing modes, flow control instructions, pseudo-instructions, procedures and runtime stack, call and return, MIPS register conventions, alternative IA-32 architecture.	Sections 2.1 – 2.9 Sections 2.13, 2.15 – 2.18 Sections 3.2 – 3.3 Appendix A.9 – A.10
4	CPU performance and metrics, CPI, performance equation, MIPS as a metric, Amdahl's law, benchmarks and performance of recent Intel processors.	Chapter 4
5 , 6	Integer multiplication, integer division, floating point representation, IEEE 754 standard, normalized and de-normalized numbers, zero, infinity, NaN, FP comparison, FP addition, FP multiplication, rounding and accurate arithmetic, FP instructions in MIPS.	Sections 3.4 – 3.6 Sections 3.8 – 3.9
7 , 8,9	Designing a processor, register transfer logic, datapath components, clocking methodology, single-cycle datapath, main control signals, ALU control, single-cycle delay, multi-cycle instruction execution, multi-cycle implementation, CPI in a multi-cycle CPU.	Sections 5.1 – 5.5
10,11	Pipelining versus serial execution, MIPS 5-stage pipeline, pipelined datapath, pipelined control, pipeline performance.	Sections 6.1 – 6.3
12,13	Pipeline hazards, structural hazards, data hazards, stalling pipeline, forwarding, load delay, compiler scheduling, hazard detection, stall and forwarding unit, control hazards, branch delay, dynamic branch prediction, branch target and prediction buffer.	Sections 6.4 – 6.6
14 , 15	Cache memory design, locality of reference, memory hierarchy, DRAM and SRAM, direct-mapped, fully-associative, and set-associative caches, handling cache miss, write policy, write buffer, replacement policy, cache performance, CPI with memory stall cycles, AMAT, two-level caches and their performance, main memory organization and performance. Virtual memory, address mapping, page table, handling a page fault, TLB, virtual versus physical caches, overlapped TLB and cache access.	Sections 7.1 – 7.6

Tentative Grading Policy and Exam Dates

- Quizzes : 6%
- Home Assignments : 4%
- Lab Assignments : 20%
- Projects : 20%

- Major Exam I : 15%

  (Sunday, 6th April, 2008 – 6.30pm to 8.30pm)

- Major Exam II : 15%

  (Tuesday, 20th May, 2008 – 6.30pm to 8.30pm)

- Final Exam : 20%

  (Tuesday, 10th June 2008 – 7.30 am to 10.30am)

Contact Details :

Room Number : 22/313
E-mail : arnaseer@kfupm.edu.sa

Office Hours :

Saturday, Sunday & Tuesday: **12.15 PM to 1.00 PM**

Software Tools used in Lab/Projects

- **PCSpim simulator**: runs MIPS-32 assembly language programs

(PCSPIM – A MIPS32 Simulator can be downloaded from http://www.cs.wisc.edu/~larus/spim.html,

Also refer Appendix A in Patterson and Hennessy Text Book)

- **MARS Simulator**: runs MIPS-32 assembly language programs (visit MARS homepage)

- **Logisim Simulator**: educational tool for designing and simulating CPUs (visit Logisim homepage)

Attendance Policy

- **Because absence from class will prevent a student from getting the full benefit of a course, and because in many courses each student's involvement contributes to the learning process for all other students in the class, attendance is mandatory for every exercise of a course in which a student is registered. Excessive absences may result in withdrawal from the class.**

- **A regular student should attend all classes and laboratory sessions. A student may be discontinued from a course and denied entrance to the final examination if his attendance is less than the limit determined by the University Council.**

- **A regular student will not be allowed to continue in a course and to take the final examination and will be given a DN grade if his unexcused absences are more than 20% of the lecture and laboratory sessions scheduled for the course (Refer Undergraduate Bulletin – *section on Attendance and withdrawal from study pp. 25-27* for more details)**

Academic Dishonesty Policy

- **In order for instructors to fairly assess the quality and quantity of a student's learning (through course grades) as determined by work that students represent as their own, a relationship of trust between instructor and student is essential. Because violations of academic integrity most often involve, but are not limited to, efforts to deceive instructors, they represent a breach of the trust relationship between instructor and student, and undermine the core values of the university.**

- **For these reasons, the University and its instructors treat issues of academic dishonesty as serious violations of academic trust, and conduct rigorous investigations of students suspected of committing such acts.**

ACTS OF ACADEMIC DISHONESTY INCLUDE, BUT ARE NOT LIMITED TO, THE FOLLOWING:

- the illegitimate use of materials in any form during a quiz or examination
- copying answers from the quiz or examination paper of another student
- plagiarizing (submitting as one's own ideas the work of another) or falsifying materials or information used in the completion of any assignment which is graded or evaluated as the student's individual effort
- submitting the same work for more than one course without the consent of the instructors of each course in which the work is submitted
- copying material from a web page and submitting it as one's own work
- quoting extensively from a document without making proper references to the source

❑ **If a student is found committing such acts in a quiz or home assignment or exam or term paper, he will be given a grade 0 in that part of the course.**

Academic Calendar Second Semester 2007-2008 (072)

Wk	Saturday	Sunday	Monday	Tuesday	Wednesday
1	Feb 16 Classes Begin	Feb 17	Feb 18	Feb 19 Last day for adding	Feb 20
2	Feb 23	Feb 24	Feb 25	Feb 26 Last day dropping without W	Feb 27
3	Mar 1	Mar 2	Mar 3	Mar 4 Quiz 1	Mar 5
4	Mar 8	Mar 9	Mar 10	Mar 11	Mar 12
5	Mar 15	Mar 16	Mar 17	Mar 18	Mar 19
6	Mar 22	Mar 23 Quiz 2	Mar 24	Mar 25 Midterm warning	Mar 26
7	Mar 29	Mar 30 Home Assignment 1 Submission	Mar 31	Apr 1 Last day dropping with W	Apr 2
8	Apr 5	Apr 6 Major Exam I	Apr 7	Apr 8	Apr 9
9	Apr 12	Apr 13 Midterm Break	Apr 14	Apr 15	Apr 16
10	Apr 19	Apr 20	Apr 21	Apr 22 Project 1 Submission	Apr 23
11	Apr 26	Apr 27 Quiz 3	Apr 28	Apr 29 Last day dropping all courses with W	Apr 30
12	May 3 Early registration 073,081,Coop	May 4	May 5	May 6	May 7
13	May 10	May 11 Home Assignment 2 Submission	May 12	May 13	May 14
14	May 17	May 18 Quiz 4	May 19	May 20 Major Exam II	May 21
15	May 24	May 25	May 26	May 27 Dropping all courses with WP/WF	May 28
16	May 31	Jun 1 Project 2 Submission	Jun 2	Jun 3	Jun 4 Last day of classes
16	Jun 7 Finals begin	Jun 8	Jun 9	Jun 10 Final Exam	Jun 11
17	Jun 14	Jun 15	Jun 16	Jun 17	Jun 18

ICS 233
Computer Architecture & Assembly Language

INTRODUCTION

Lecture Outline

- **Computing classes**
- **Computer Growth**
- **Components of a Computer System**
- **Programmer's View of a Computer System**

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Lecture 1

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Computing classes

Three Computing Classes

- **Changes in computer Usage have led to three different computing markets, each characterized by different applications, requirements, and computing technologies**

- **Desktop Computing**
- **Enterprise Servers**
- **Embedded Computers**

Desktop Computing

- Spans from low end systems to high-end heavily configured workstations
- Used for General-purpose applications
- Market tends to be driven **to optimize price-performance**
- Performance improvements must be traded off against cost
- Performance metric of interest is usually **response time**

Enterprise Servers

- Backbone of large-scale enterprise computing (to provide larger-scale and more reliable file and computing services)
- **Three critical design issues – Availability, Scalability, Throughput**
  - **Availability** means that the system can reliably and effectively provide a service (in the face of component failures, usually through the use of redundancy)
  - **Scalability** – ability to scale up the computing capacity, the memory, the storage, and the I/O bandwidth
  - **Throughput** – overall performance in terms of transactions per minute or web pages served per second
- Cost is important but not as much of a concern
- Performance is paramount, metric of interest is usually **throughput**

Embedded Computers

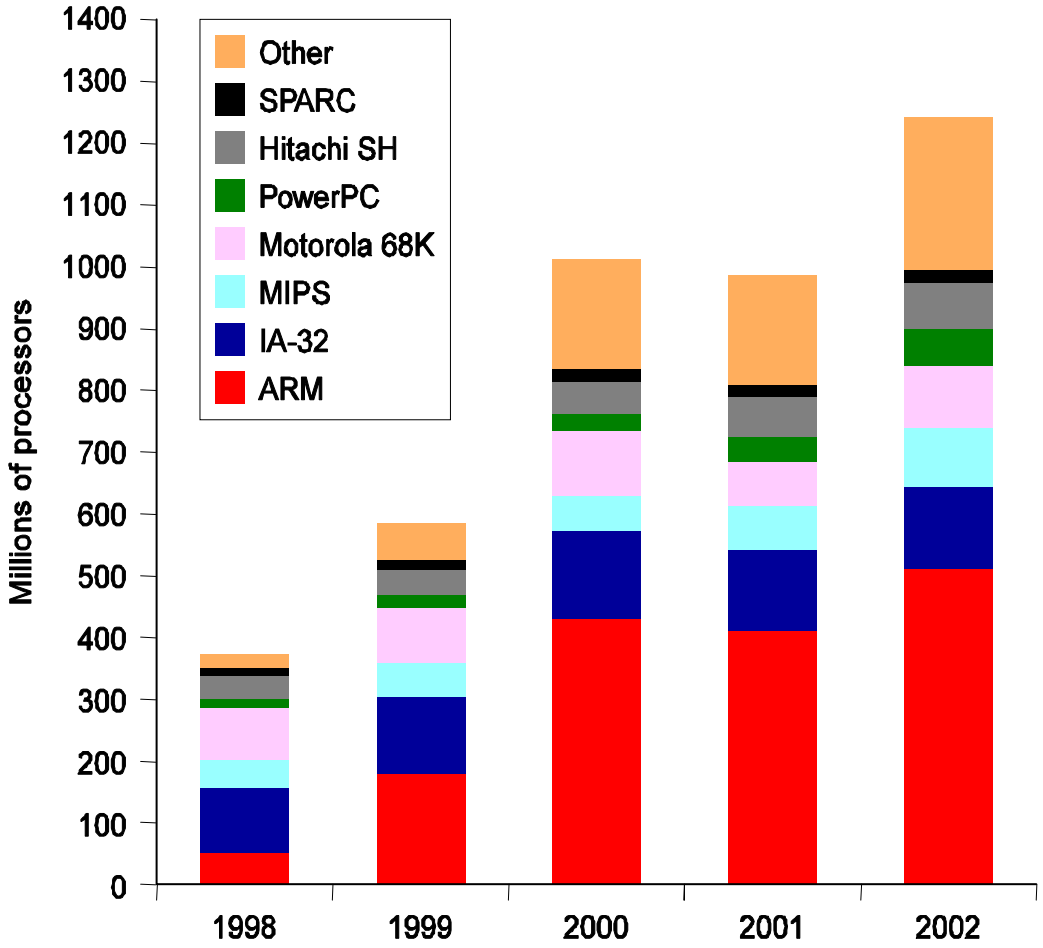
- Fastest growing portion of the Computer market
- Devices range from everyday machines (most microwave appliances, washing machines, printers, networking switches and all cars contain simple embedded microprocessors) to handheld digital devices (such as palmtops, cell phones and smart cards) to video games and digital set-up boxes
- Cost is paramount
- Need to minimize memory and power
- Requirement of Real-time performance (highly application dependent)
- Specialized applications

Three Computing System Characteristics

Feature	Desktop	Server	Embedded
System price	$1000 - $10,000	$10,000 - $10,000,000	$10 - $100,000 (including network routers at the high end)
Processor price	$100 - $1000	$200 - $2000	$0.20 - $200
Microprocessors sold per year (estimates for 2000)	150,000,000	4,000,000	300,000,000 (32-bit and 64-bit processors only)
Critical System Design issues	Price-performance, graphics performance	Throughput, availability, scalability	Price, power, application-specific performance

Microprocessor Sales (1998 – 2002)

- ARM processor sales exceeded Intel IA-32 processors, which came second
- ARM processors are used mostly in cellular phones
- Most processors today are embedded in cell phones, video games, digital TVs, PDAs, and a variety of consumer devices



Computer Sales (1998 – 2002)