Name: Id#

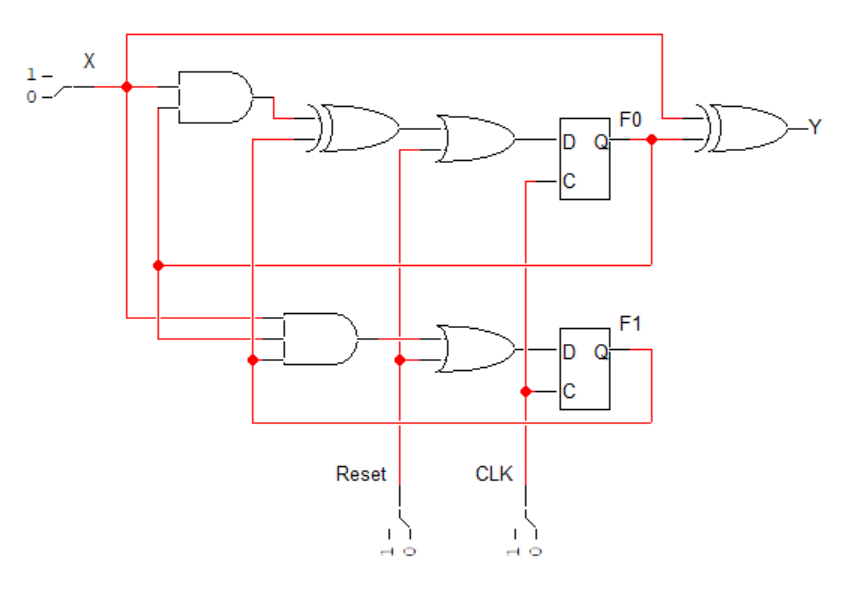
COE 202, Term 201

Digital Logic Design

Quiz# 6 Solution

Date: Sunday, Nov. 29, 2020

**Q1. [7 points]** Consider the sequential circuit given below which has input X and output Y:



1. (2 points) What is the reset state? Is the reset asynchronous or synchronous?

The reset state is F1 F0 = 1 1. The reset is synchronous.

1. (1 point) Is the circuit Mealy or Moore? Justify your answer.

It is Mealy because the output depends on the input.

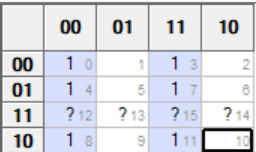
1. (4 points) Derive the state table for this sequential circuit.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Present State | | Input | Next State | | Output |
| F1 | F0 | X | F1+ | F0+ | Y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

**Q2. [7 points]** Given the state table below of a sequential circuit that has an input X and an output Y:

1. (2 points) Derive the output equation of the given sequential state table assuming asynchronous reset with the reset state being F2 F1 F0 = 0 0 0. Note that entries that are not shown represent unused states.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | | Input | Next State | | | Output |
| F2 | F1 | F0 | X | F2+ | F1+ | F0+ | Y |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |



Y = (F0 ⊕ X)’

1. (5 points) Complete the given two input/output sequences and then determine the function of the circuit.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cycle** | **0** | **1** | **2** | **3** | **4** |
| Input *x* | 1 | 1 | 0 | 0 | 0 |
| F2 | 0 | 0 | 1 | 0 | 0 |
| F1 | 0 | 1 | 0 | 1 | 1 |
| F0 | 0 | 1 | 0 | 1 | 1 |
| Output *z* | 0 | 1 | 1 | 0 | 0 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cycle** | **0** | **1** | **2** | **3** | **4** |
| Input *x* | 0 | 0 | 1 | 0 | 0 |
| F2 | 0 | 0 | 0 | 1 | 0 |
| F1 | 0 | 0 | 1 | 0 | 1 |
| F0 | 0 | 1 | 0 | 0 | 1 |
| Output *z* | 1 | 0 | 0 | 1 | 0 |

The circuit is implementing the equation Y= 3X – 3 = 3(X-1).